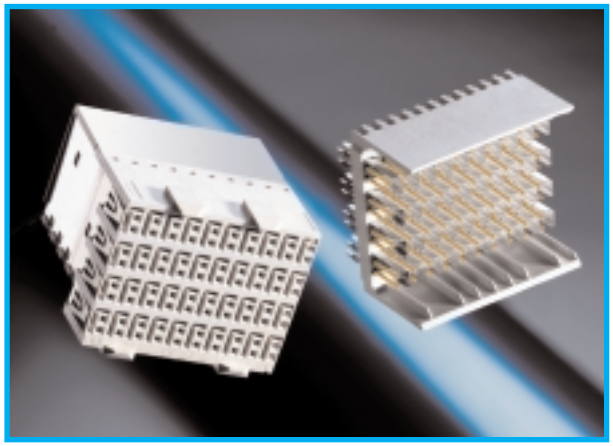
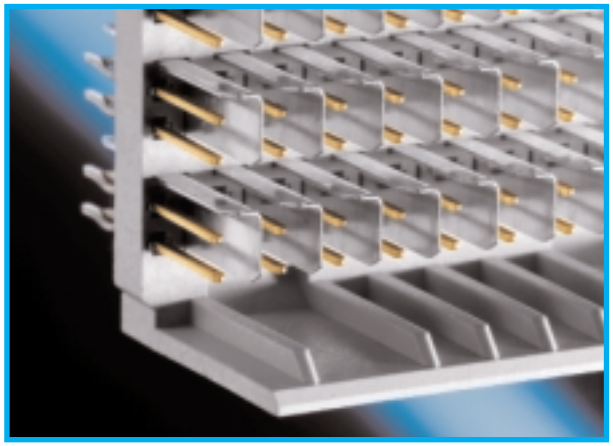
ERmet ZD
High Speed Differential Hard Metric Connector System





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Proposal for a System Simulation including the ERNI ERmet ZD Connector

This is a proposal for a system simulation scenario of a high speed data communication backplane system. The goal of this investigation is to demonstrate the feasibility of the ERNI ERmet ZD connector to provide an interface with a superior electrical behavior.

The influence of several design alternatives with respect to the ERNI ERmet ZD connector and the printed circuit board will be evaluated:

- distance between daughter cards
- connector to board interface
- width of transmission lines
- PCB material
- metalization layer in the PCB
- termination of the transmission lines
- type of transmission lines

The simulation configuration will be explained in detail on the following pages.

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Table of Content

1 System configuration 3
1.1 Point-to-point connection 3
1.2 Connector to board interface 4

2 Layout considerations 5
2.1 Width of transmission lines 5
1.2 PCB material 5
1.3 Layer of striplines 6
1.4 Variance in the impedance of termination resistors and of transmission lines 7
1.5 Type of transmission lines (microstrip, stripline) 7

3 Summary of simulation setups 8
3.1 Simulation experiment for FR4 PCB material 8
3.2 Simulation experiment for Rogers 4350 PCB material 9
3.3 Simulation results 10
3.3.1 Simulation analyses with nominal device parameters 10
1.1.2 Simulation analyses with variation of the external termination resistance and the transmission line width 10
1.1.3 Simulation run with variation of the on chip termination resistance and the transmission line width 10
1.4 Comments on design alternatives 11

2 Circuit descriptions for simulation 12
2.1 Circuit description of backplane system 12
2.2 Analysis setup 13
2.2.1 Eye diagrams 13
2.2.2 Typical impedance 14
2.2.3 S-parameter 15

1 System configuration

1.1 Point-to-point connection

The following general system scenario is used for this simulation study:

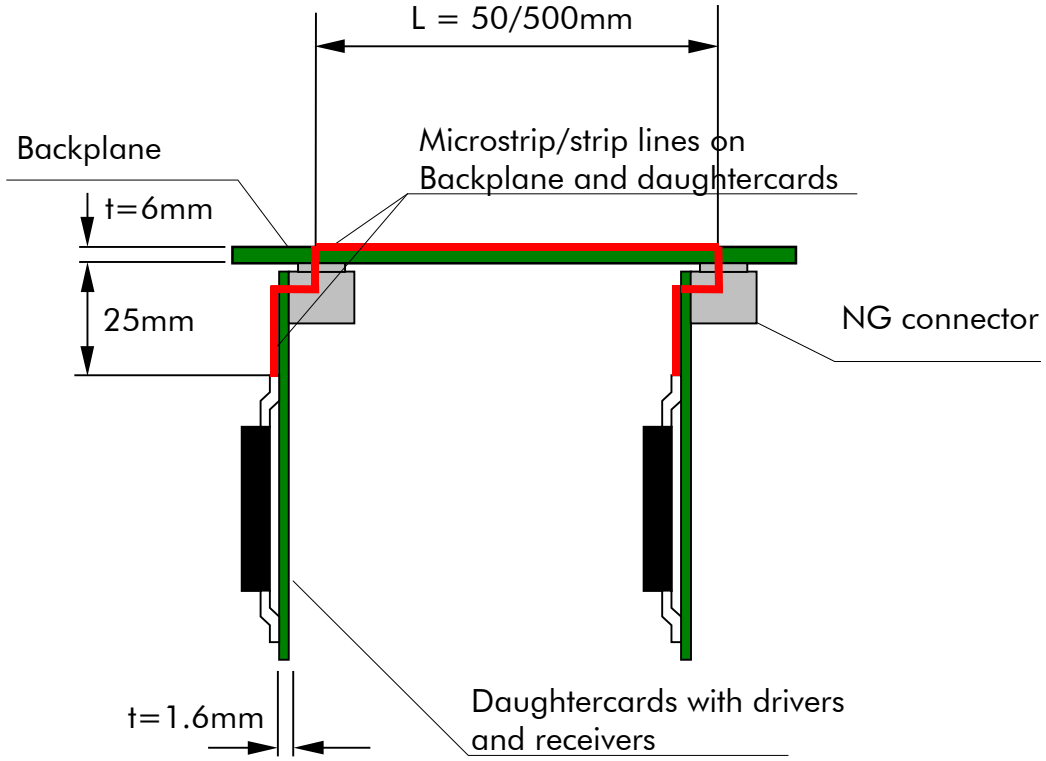


Fig. 1 System configuration

The signal path is a point-to-point connection between two integrated circuits on two different daughter cards. The daughter cards are plugged into a backplane printed circuit board. The connections are done using the ERNI ERmet ZD connector. The analysis is done for two different track lengths on the backplane:

Track length L [mm]	L_1	L_2
L	50	500

Characteristic impedance of differential striplines Z_{wdiff} = 100 Ω
Data rate: 2.4Gb/s and 4.8Gb/s using a Non-Return Zero (NRZ) 8B10B code.

1.2 Connector to board interface

Three different connector to board interface scenarios of the ERNI ERmet ZD connector will be analyzed. The pictures in Fig. 2 shows the two design alternatives which will be available for the connector. Now the following combinations are evaluated during the simulation study:

Connector to board interface	CBI_1	CBI_2	CBI_3
Backplane (male connector)	pressfit	SMD	pressfit
Daughtercard (female connector)	pressfit	SMD	SMD

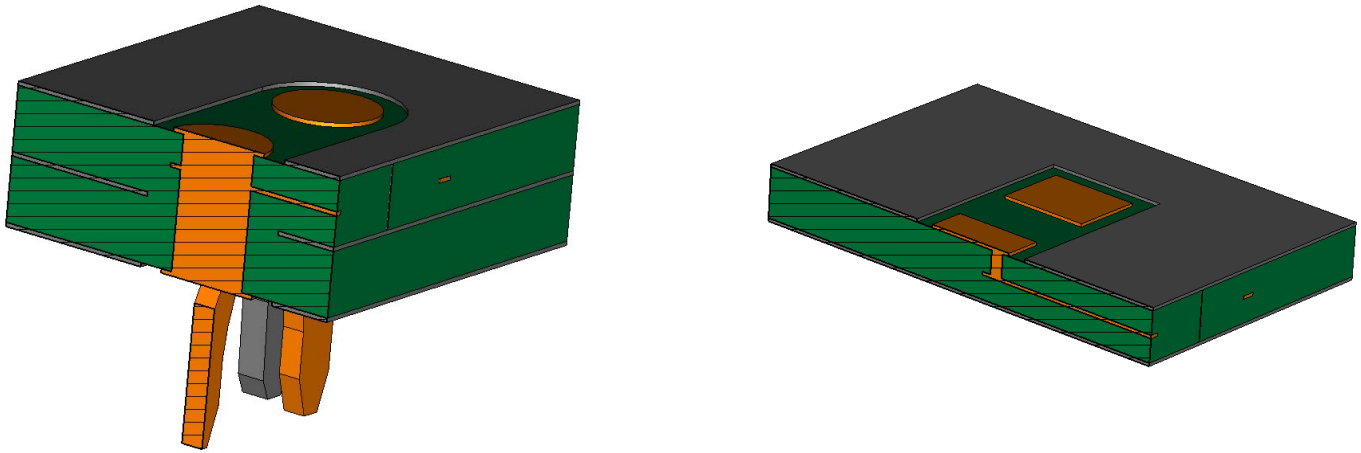


Fig. 2 Connector to board interfaces: pressfit pins - SMD pins

2 Layout considerations

2.1 Width of transmission lines

The transmission lines on the backplane will be simulated using three design alternatives with different line widths W of a single track. Depending on the selected width W, the given differential impedance Z_d = 100Ω, the selected material (ε_r), and the minimum distance d, the thickness b of the insulation layers must be adjusted.

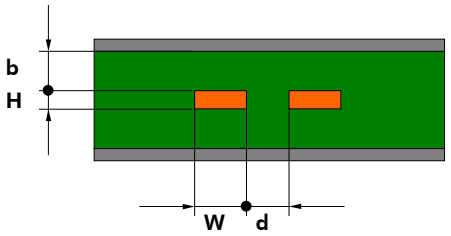


Fig. 3 Transmission line dimensions

Width of lines [mm]	W_1	W_2	W_3
W	0.15	0.2	0.25

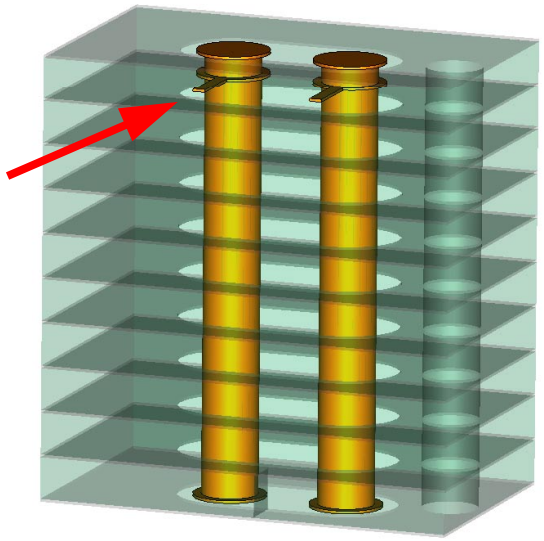
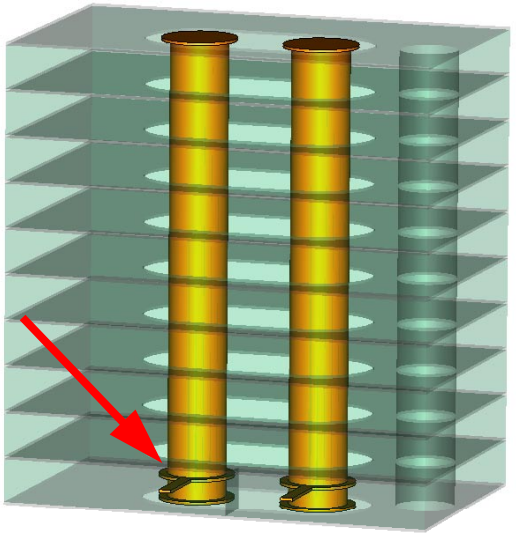
2.2 PCB material

Three different PCB materials with different electrical properties are evaluated:

PCB Material properties	ε_r	tan δ
FR4	4.5	0.02
Gigaver /Rogers 4350	3.5	0.004

2.3 Layer of striplines

The influence of routing of the striplines in several metal layers in the backplane will be evaluated. A difference in electrical behavior is expected due to different connections of the striplines to the vias of the pressfit pins. Due to technological reasons, the routing for SMD pins will only be done in the upper layers of the backplane PCB.

Metal layer in backplane	**Layer_1**	**Layer_2**
Layer	highest inside the board	lowest inside the board
		

2.4 Variance in the impedance of termination resistors and of transmission lines

The termination of the transmission lines in such a system can be done in two ways:

- on the PCB using disrete SMD resistors
- in the receiver circuit using on-chip doped resistors

In addition, the typical impedance of the transmission lines has a certain tolerance due to manufacturing tolerances. In this simulation example, these tolerances are represented by a variation of the width of the lines.

Depending on process variations of the selected technology, the influence of the termination and its variation on the overall system behavior will be evaluated:

Manufacturing tolerances	tolerance
SMD resistors	+/- 2%
On-chip doped resistors	+/- 15%
Transmission line width	+/- 5%

2.5 Type of transmission lines (microstrip, stripline)

The transmission lines can be implemented as microstrip lines (at the surface of the PCB) or as strip lines (in the inner layers of the PCB). The difference in electrical behavior is shown in a one certain simulation

3 Summary of simulation setups

The design alternatives shown in the previous chapters are now combined in the following ways:

3.1 Simulation experiment for FR4 PCB material

The first simulation block evaluates the system behavior for FR4 PCB material.
Please note, that only trace widths of 0.15mm and 0.2mm have been used. The reason was, that a trace width of 0.25mm together with a maximum trace spacing of 0.4mm would result in a thickness of the insulator between the two ground layers of more than 0.8mm.
It is assumed, that such a thickness cannot be implemented in a standard backplane.

	Connector to board interface		**PCB**	**Backplane**			
Simulation run	**Backplane**	**Daughter-card**	**Material**	**Trace length [mm]**	**Trace width [mm]**	**Backplane transmission line type**	**Layer of transmission line**
1	PF	PF	FR4	500	0.15	stripline	top
2	PF	SMD	FR4	500	0.15	stripline	top
3	PF	PF	FR4	500	0.15	stripline	bottom
4 *)	PF	SMD	FR4	500	0.15	stripline	bottom
5 *)	PF	PF	FR4	500	0.2	stripline	top
6 *)	PF	SMD	FR4	500	0.2	stripline	top
7 *)	PF	PF	FR4	500	0.2	stripline	bottom
8 *)	PF	SMD	FR4	500	0.2	stripline	bottom
9	PF	PF	FR4	50	0.15	stripline	top
10	PF	SMD	FR4	50	0.15	stripline	top
11	PF	PF	FR4	50	0.15	stripline	bottom
12	PF	SMD	FR4	50	0.15	stripline	bottom
13 *)	PF	PF	FR4	50	0.2	stripline	top
14 *)	PF	SMD	FR4	50	0.2	stripline	top
15 *)	PF	PF	FR4	50	0.2	stripline	bottom
16 *)	PF	SMD	FR4	50	0.2	stripline	bottom

*) These simulations are only available in the extended report.

3.2 Simulation experiment for Rogers 4350 PCB material

The same simulation experiment is carried out for Rogers 4350 PCB material. In this case, trace widths of 0.25 mm results in a lower thickness of the insulator and can be implemented.

	Connector to board interface		**PCB**	**Backplane**			
Simulation run	**Backplane**	**Daughter-card**	**Material**	**Trace length [mm]**	**Trace width [mm]**	**Backplane transmission line type**	**Layer of transmission line**
17	SMD	SMD	Rogers	500	0.15	Stripline	top
18	PF	SMD	Rogers	500	0.15	Stripline	top
19 *)	SMD	SMD	Rogers	500	0.2	Stripline	top
20 *)	PF	SMD	Rogers	500	0.2	Stripline	top
21	SMD	SMD	Rogers	500	0.25	Stripline	top
22	PF	SMD	Rogers	500	0.25	Stripline	top
23	SMD	SMD	Rogers	50	0.15	stripline	top
24	PF	SMD	Rogers	50	0.15	stripline	top
25 *)	SMD	SMD	Rogers	50	0.2	stripline	top
26 *)	PF	SMD	Rogers	50	0.2	stripline	top
27 *)	SMD	SMD	Rogers	50	0.25	stripline	top
28 *)	PF	SMD	Rogers	50	0.25	stripline	top
29 *)	SMD	SMD	Rogers	500	0.2	microstrip	top
30 *)	PF	SMD	Rogers	500	0.2	microstrip	top
31	PF	SMD	Rogers	500	0.25	Stripline	bottom
32	PF	SMD	Rogers	50	0.25	stripline	bottom

*) These simulations are only available in the extended report.

3.3 Simulation results

For every simulation run, the following analyses are performed:

3.3.1 Simulation analyses with nominal device parameters

S-parameters in the frequency domain
- magnitude of S11 of the differential signal in dB
- magnitude of S21 of the differential signal in dB
- phase of S21 of the differential signal in degrees
- |S11| and |S21| at certain frequency points in dB and in linear representation in a data table

Time domain
- Typical impedance of the overall system in Ω.
- Eye diagrams for a data transmission rate of 2.5Gbit/s and 5.0Gbit/s.

3.3.2 Simulation analyses with variation of the external termination resistance and the transmission line width

In this analysis, the following 4 combinations of process tolerances are evaluated and represented together with the nominal results:

SMD resistors	+ 2%	+ 2%	- 2%	- 2%
Transmission line width	+ 5%	- 5%	+5%	- 5%

These results are shown:
- magnitude of S11 of the differential signal in dB
- Eye diagrams for a data transmission rate of 2.5Gbit/s and 5.0Gbit/s.

3.3.3 Simulation run with variation of the on chip termination resistance and the transmission line width

In this analysis, the following 4 combinations of process tolerances are evaluated and represented together with the nominal results:

On chip doped resistors	+ 15%	+ 15%	- 15%	- 15%
Transmission line width	+ 5%	- 5%	+5%	- 5%

These results are shown:
- magnitude of S11 of the differential signal in dB
- Eye diagrams for a data transmission rate of 2.5Gbit/s and 5.0Gbit/s.

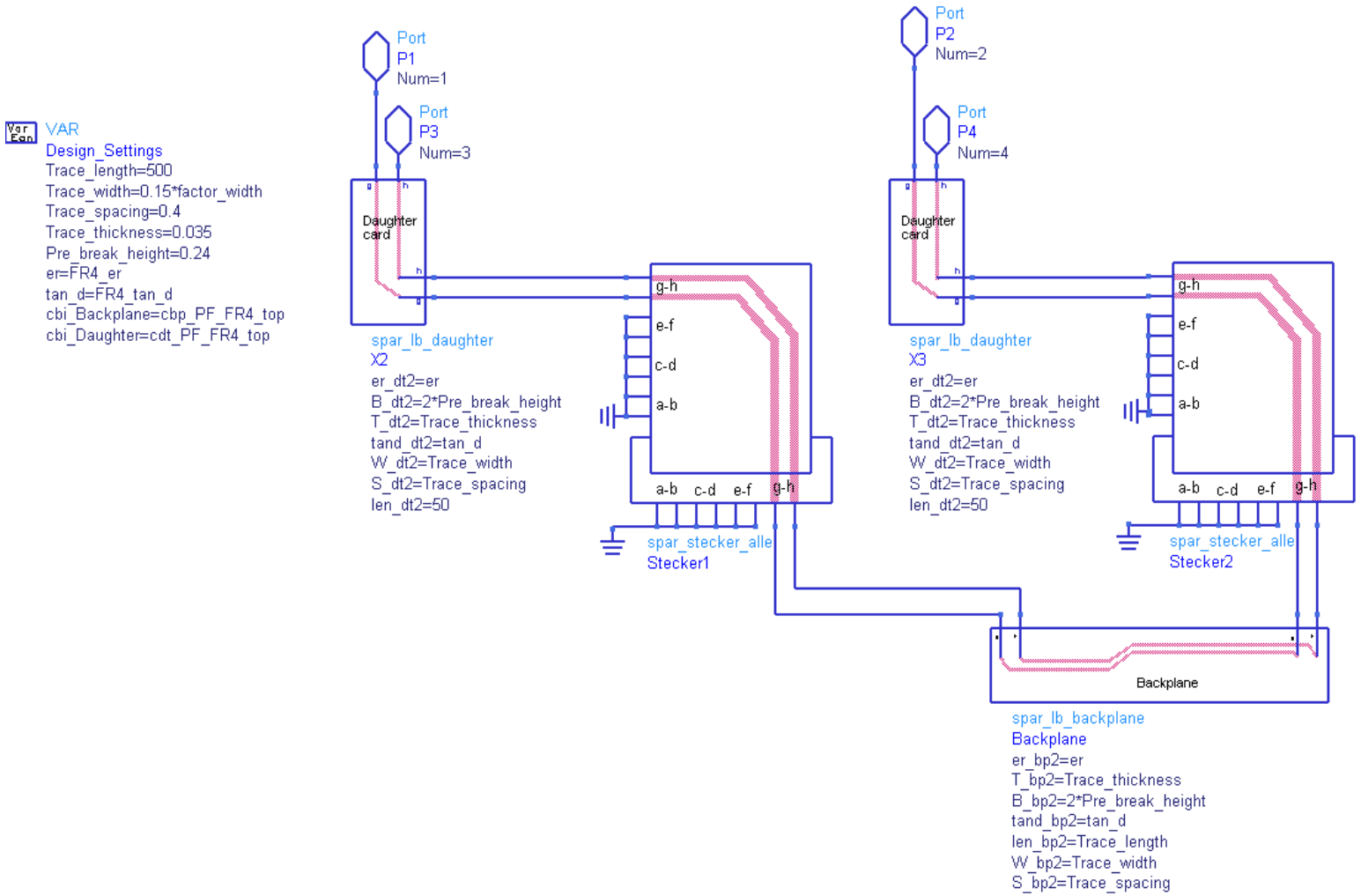
3.4 Comments on design alternatives

Please find below some comments about the described design alternatives:

Simulation setups	Comment
1, 2, 3	These 3 simulations show the typical behavior of a very lossy signal path with a large length of 500mm on a classic FR4 backplane board. Due to these heavy losses (roughly -6dB at 1.2GHz) the different design alternatives gives very similar results in the eye diagram and in the reflection behavior.
9, 10, 11, 12	This group of simulation is the same setup than above with the only exception, that the length of the signal path is reduced to 50mm instead of 500mm. Now, the losses in the FR4 backplane board are substantially lower and the influence of the different design alternatives can be seen more clearly. It can be identified, that the metalization layer on the backplane has a major influence onto the signal quality. Having the striplines on the lowest layer avoids a lot of parasitic capacitance due to the pressfit pins of the connector.
17, 18	These both simulations compare the influence of the board - to - connector interface for a long signal path of 500mm in a more advanced PCB material (Rogers 4350). Now the PCB material is no longer the ultimate bottleneck in the system performance and the difference between a fully SMT design compared to a mixed SMT / pressfit design of the connector can be seen very clearly at the eye diagrams for a transmission rate of 4.8 Gbit / s.
21, 22	This is the same setup than 17/18 for a different width of the transmission lines.
23, 24	This is a similar setup than 17/18 with the exception, that the trace length in the backplane is now only 50mm. Again, the difference between a fully SMT design compared to a mixed SMT / pressfit design of the connector can be seen very clearly at the eye diagrams for a transmission rate of 4.8 Gbit / s.
31, 32	Here, the striplines on the backplane are placed in the lowest metalization layer. The results of simulation run #31 should be compared to run #22, where the metalization layer in the backplane is in the top level (also run #32 versus run #24). The comparison shows, that the signal quality for a pressfit connector on the backplane can be improved when the lowest metalization layer is used for the stripline to reduce influence of the parasitic capacitance of the pressfit pins.

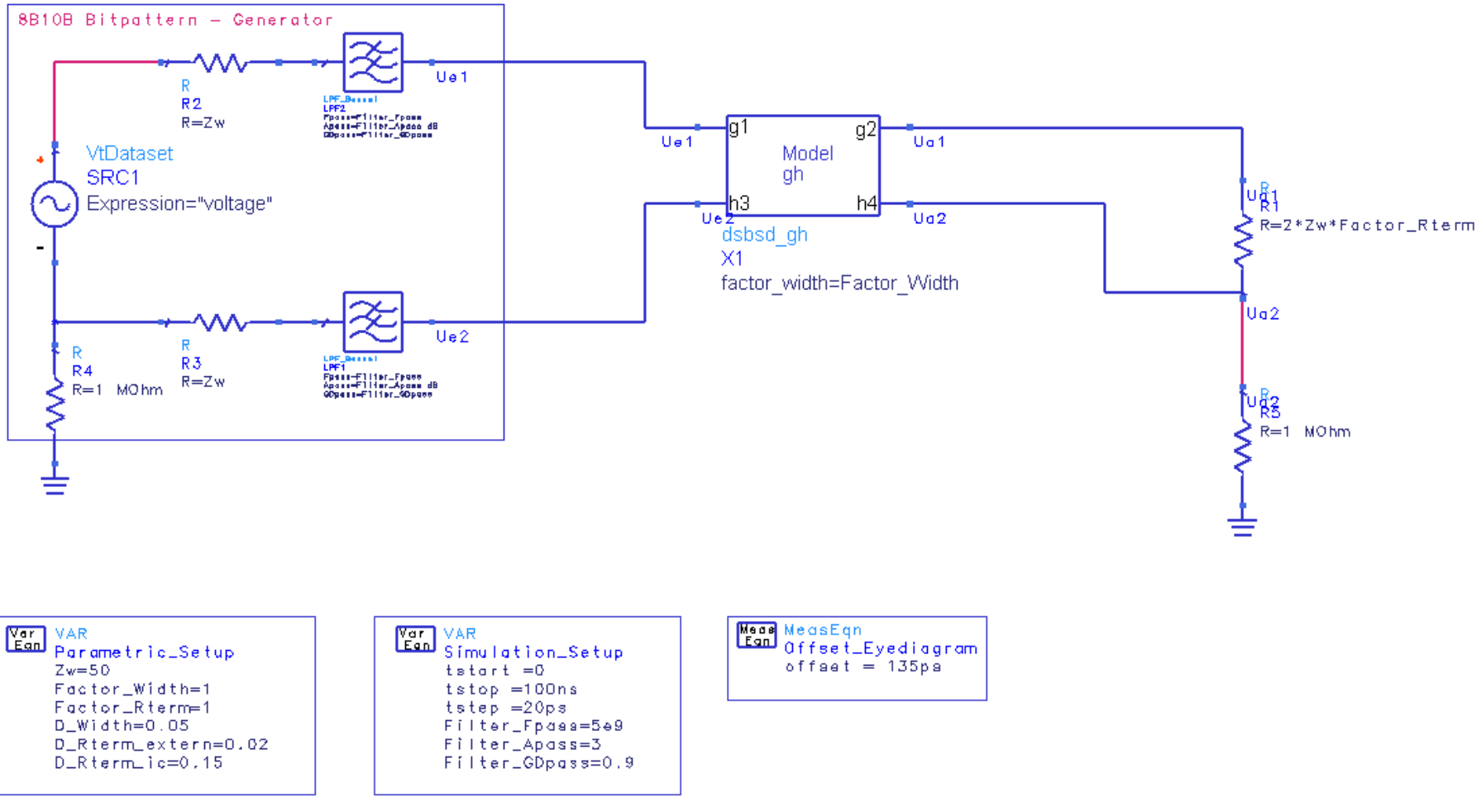
4 Circuit descriptions for simulation

4.1 Circuit description of backplane system



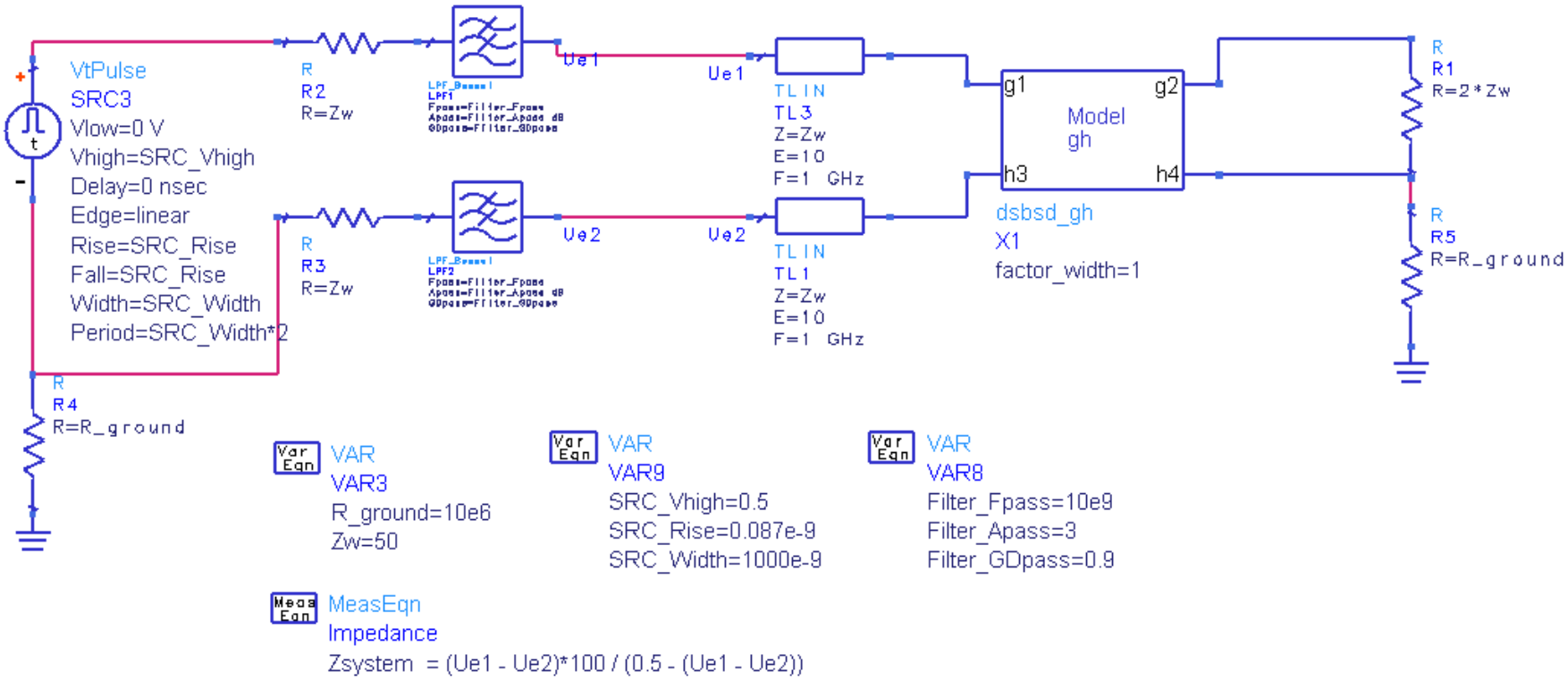
4.2 Analysis setup

4.2.1 Eye diagrams

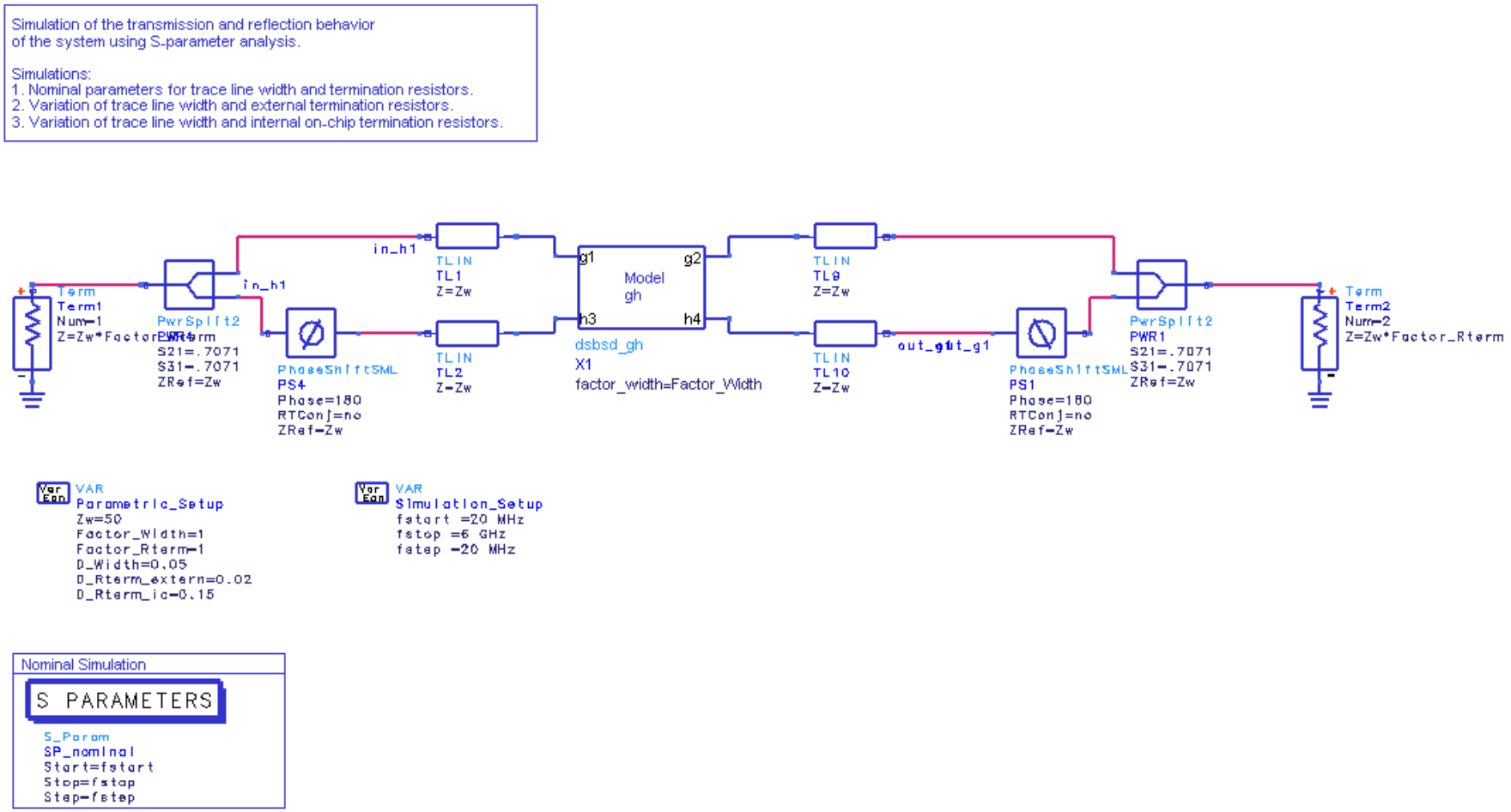


For the eye pattern generation, a 8B10B bit pattern generator is used. The bit stream, which is generated from 130 randomly selected bytes, is strored in a dataset,. This data set controls the voltage source in the bit pattern generator. The rise times (10% .. 90%) for the two different data rates are: 75ps for 4.8GBit/s and 150ps for 2.4GBit/s.

4.2.2 *Typical impedance*



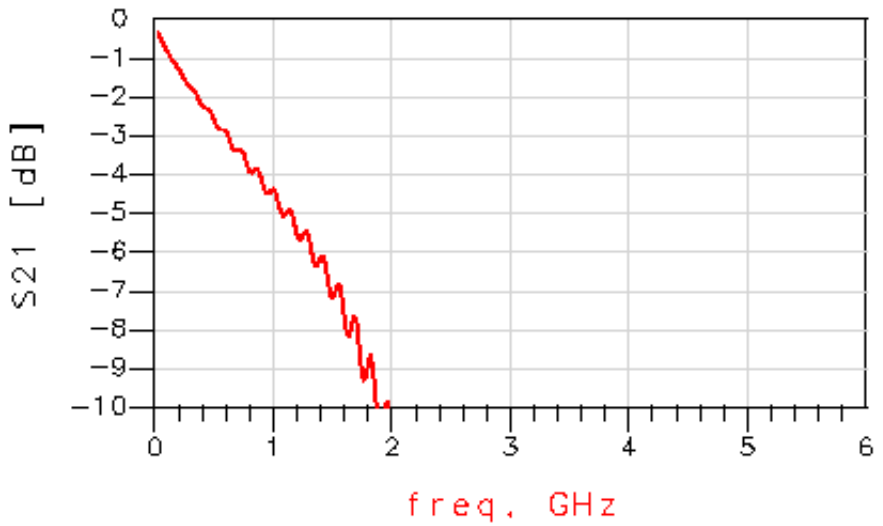
4.2.3 *S-parameter*



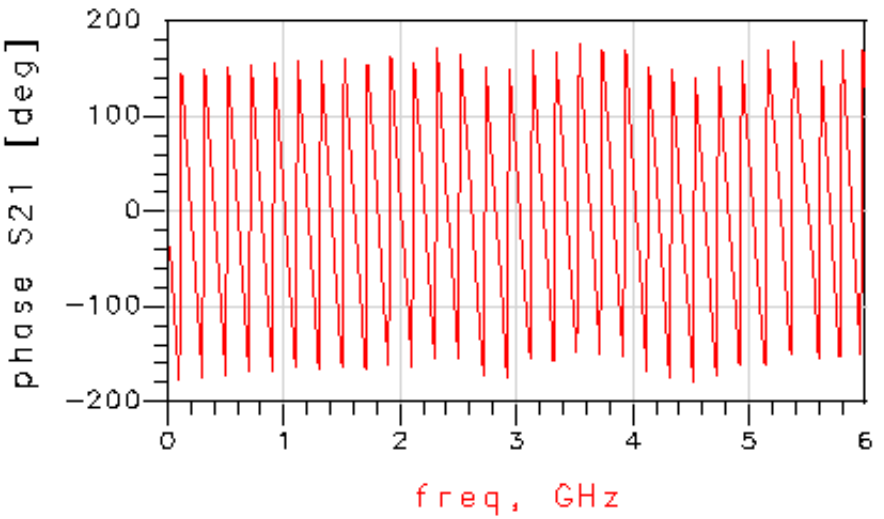
print results next results

	Connector to board interface		PCB	Backplane			
Simulation run	Backplane	Daughter-card	Material	Trace length [mm]	Trace width [mm]	Backplane transmission line type	Layer of transmission line
1	PF	PF	FR4	500	0.15	stripline	top

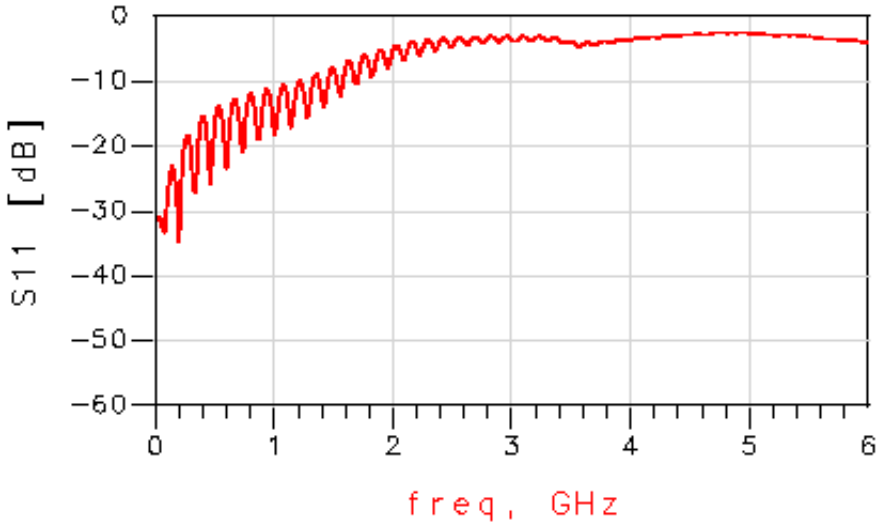
Nominal results



Magnitude of forward transmission S21



Phase of forward transmission S21



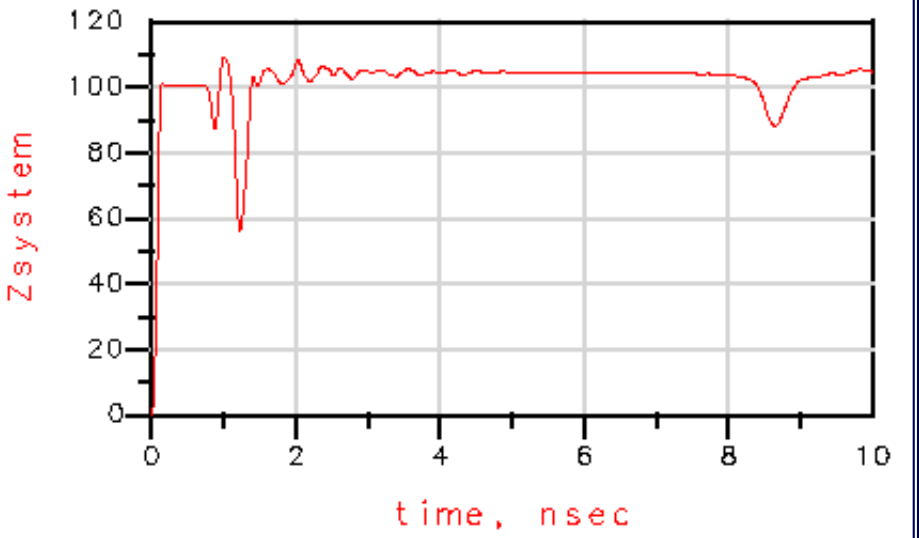
Input reflection S11

Input reflection S11

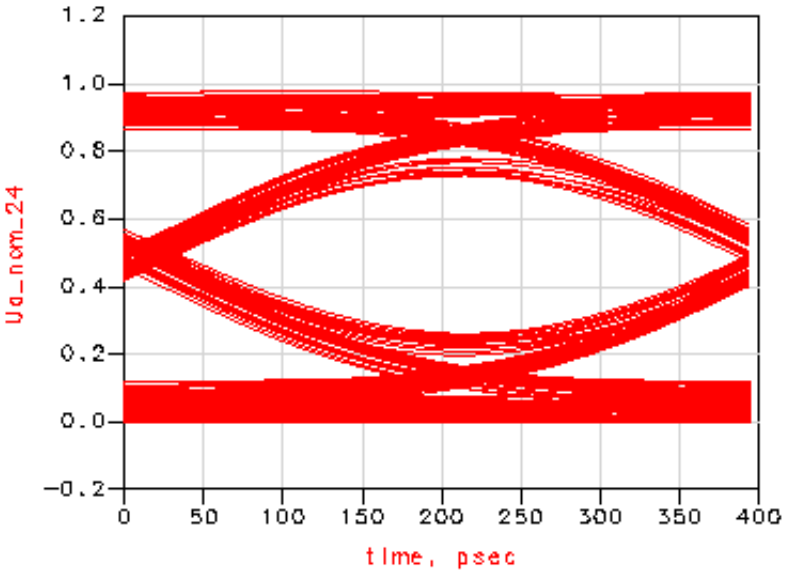
freq	S11_dB	S11_lin
1.20GHz	−10.13	0.31
2.40GHz	−3.74	0.65
3.60GHz	−4.31	0.61
4.80GHz	−2.61	0.74

Transmission S21

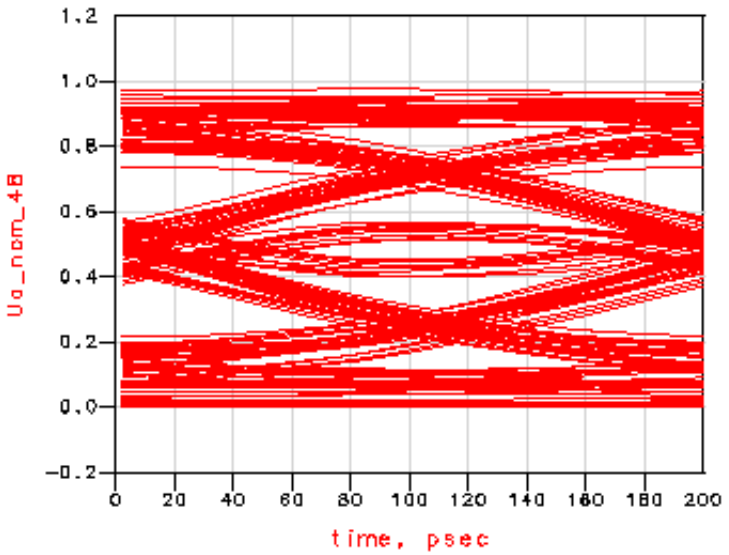
freq	S21_dB	S21_lin
1.20GHz	−5.56	0.53
2.40GHz	−15.59	0.17
3.60GHz	−23.85	0.06
4.80GHz	−47.65	4.15E−3



Impedance of transmission path

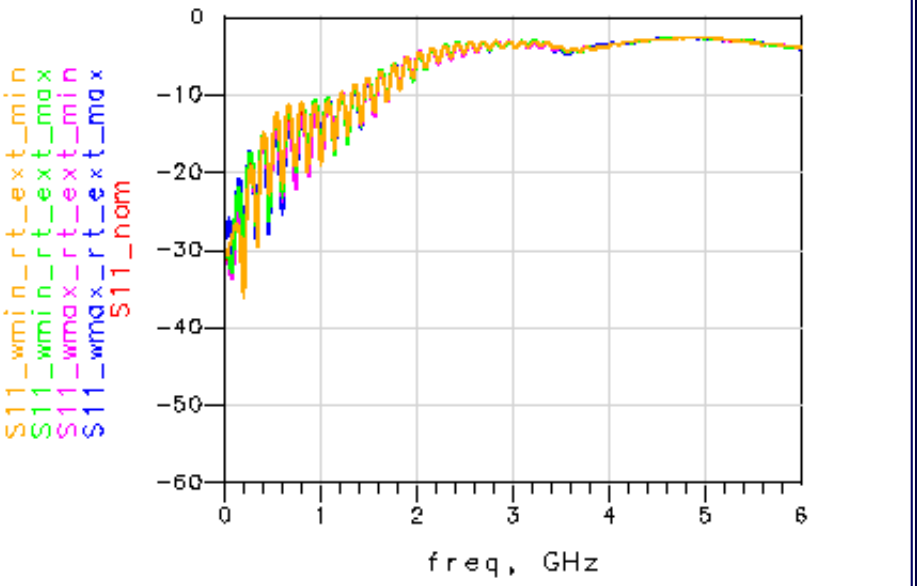


System eye diagram @ 2.4 GBit/s

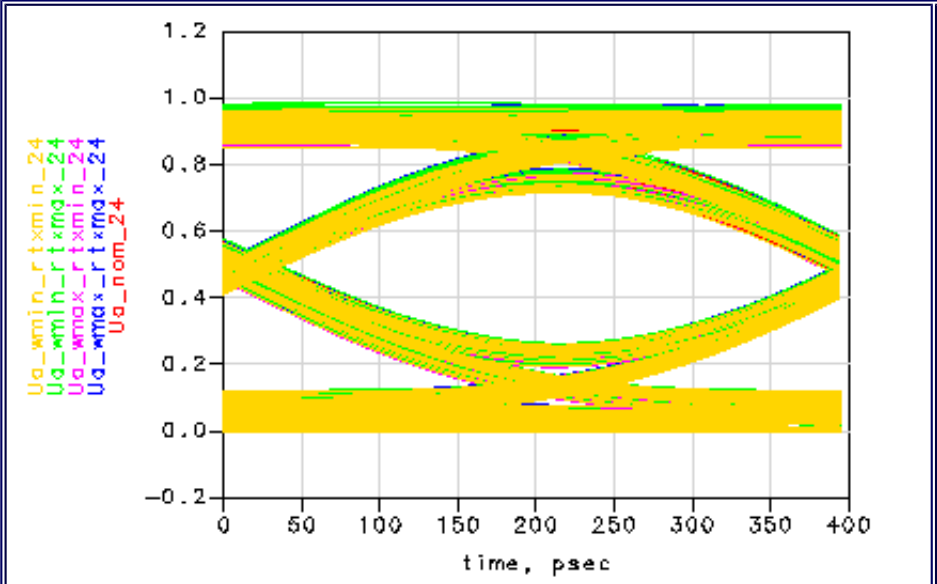


System eye diagram @ 4.8 GBit/s

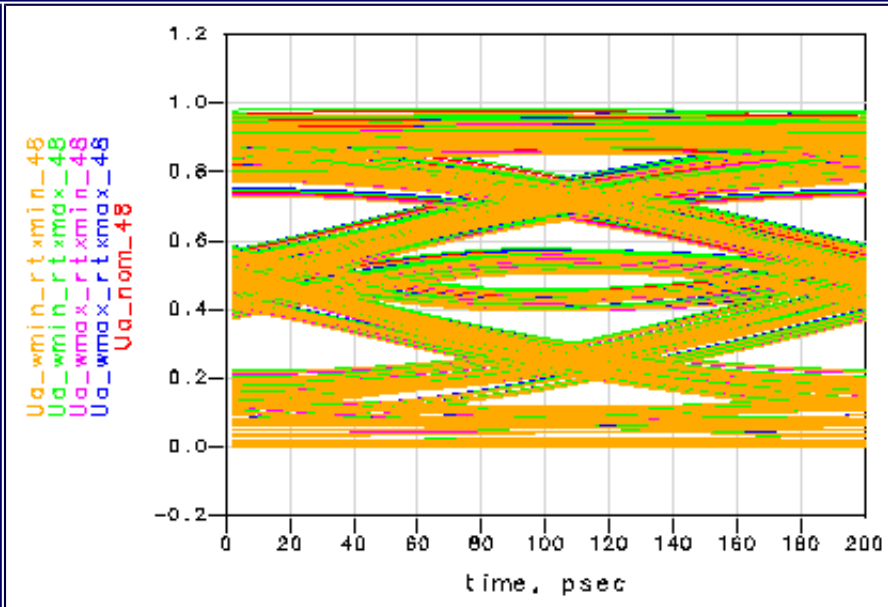
Tolerance analysis with external resistors (+/- 2%)



Input reflection S11

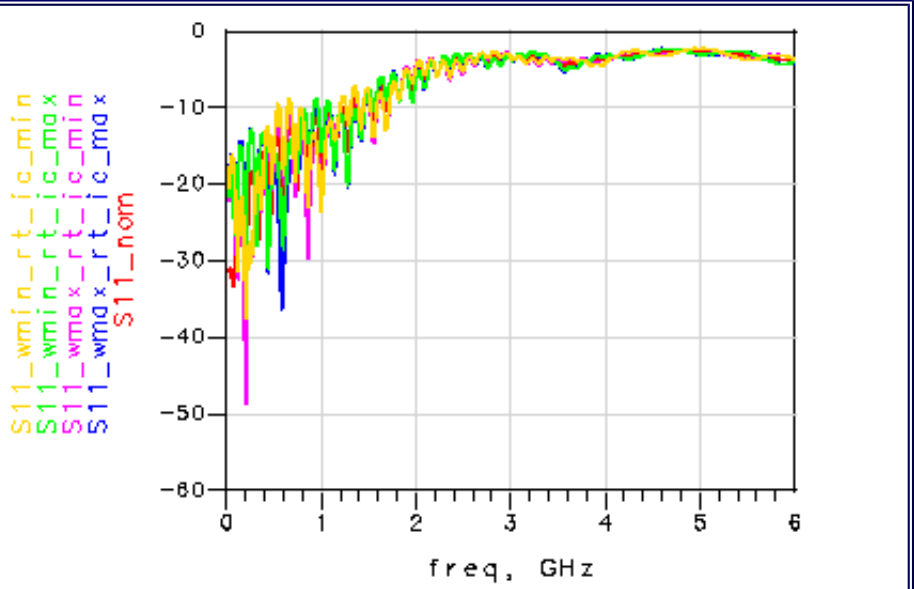


System eye diagram @ 2.4 GBit/s

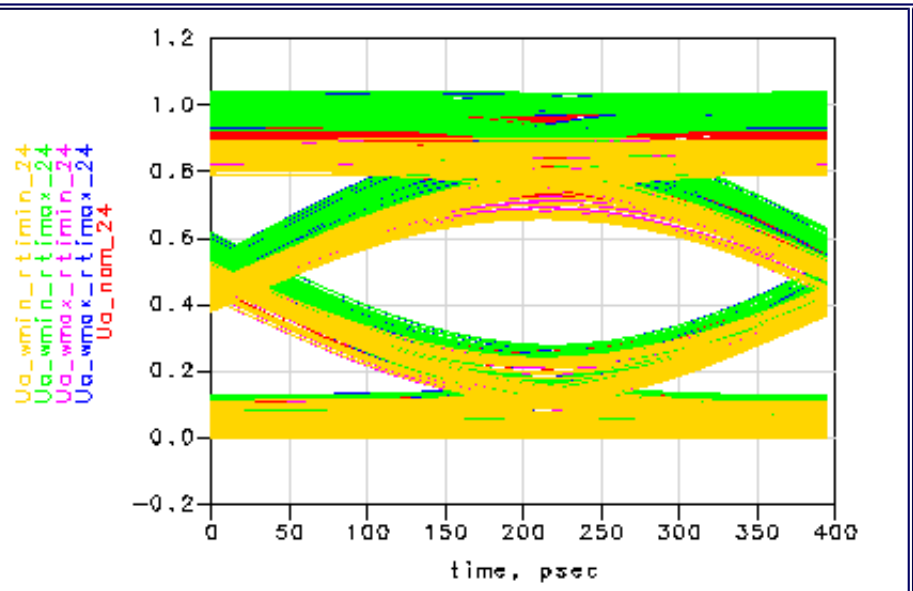


System eye diagram @ 4.8 GBit/s

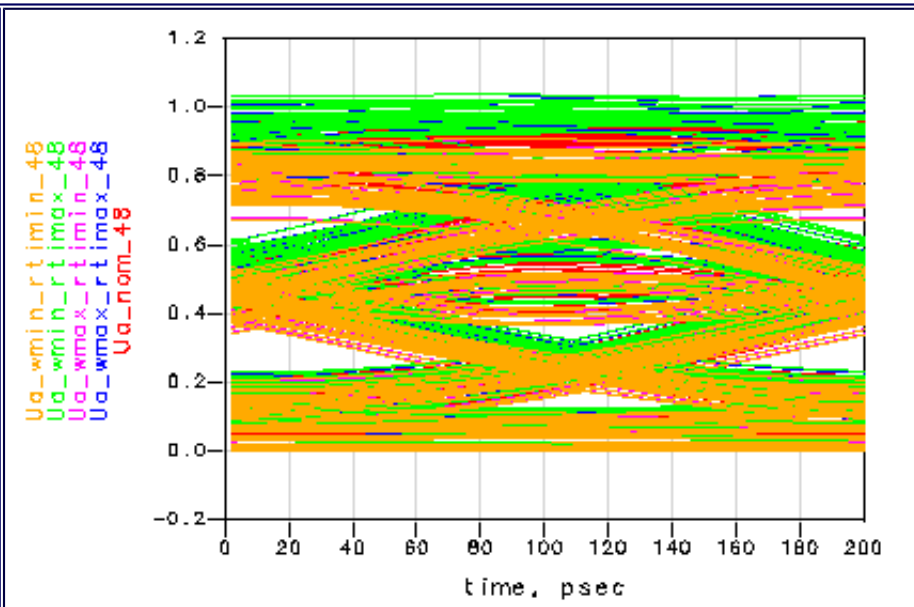
Tolerance analysis with on-chip termination resistors (+/- 15%)



Input reflection S11



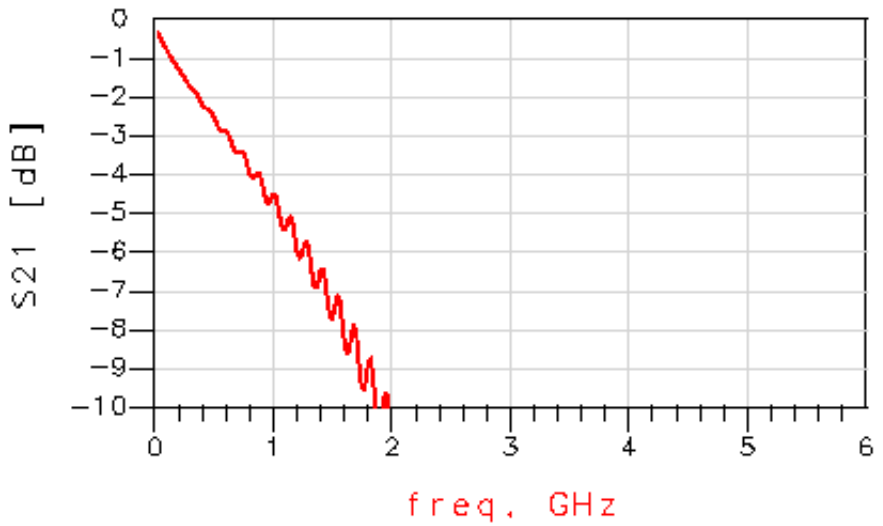
System eye diagram @ 2.4 GBit/s



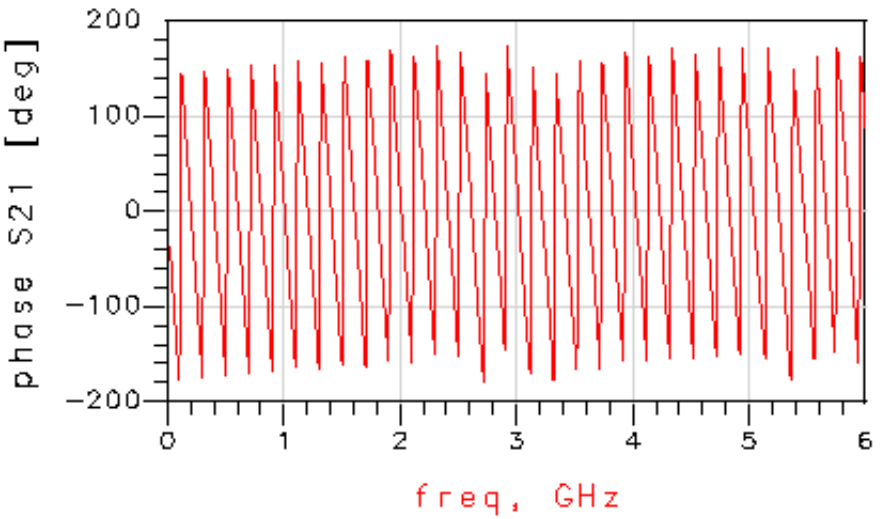
System eye diagram @ 4.8 GBit/s

	Connector to board interface		PCB	Backplane			
Simulation run	Backplane	Daughter-card	Material	Trace length [mm]	Trace width [mm]	Backplane transmission line type	Layer of transmission line
2	PF	SMD	FR4	500	0.15	stripline	top

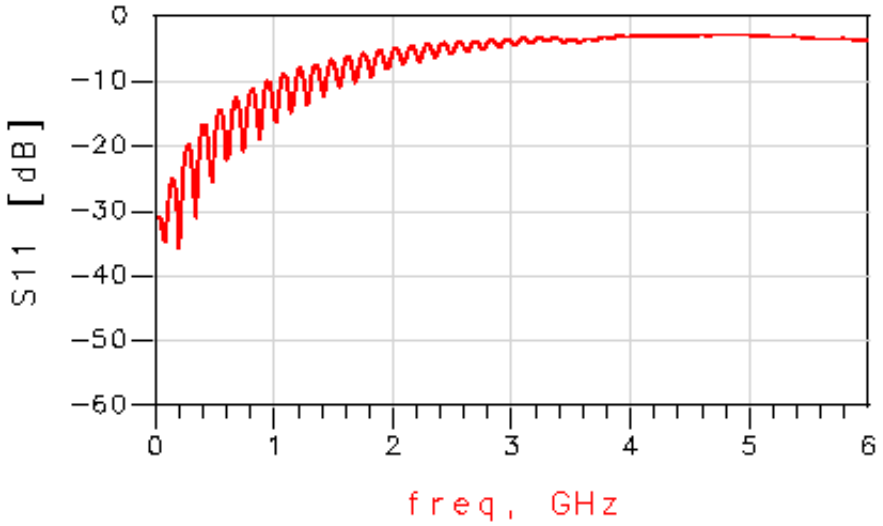
Nominal results



Magnitude of forward transmission S21



Phase of forward transmission S21



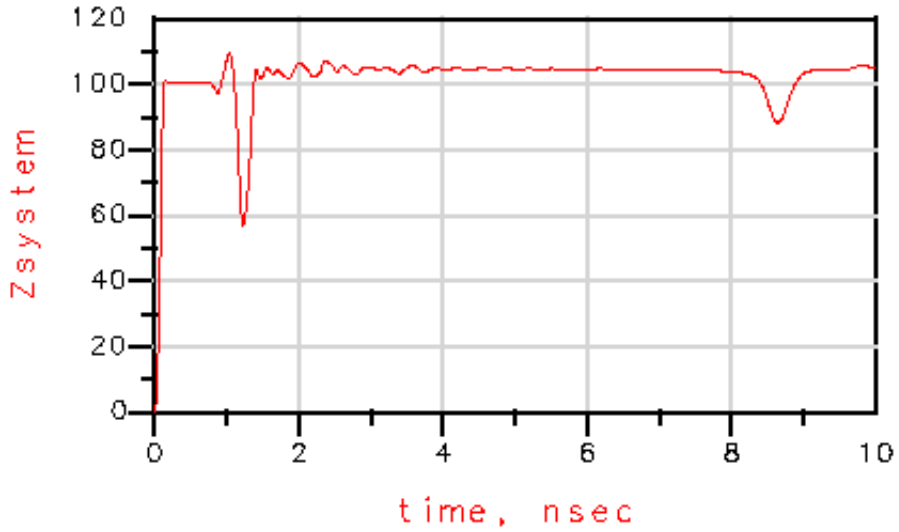
Input reflection S11

Input reflection S11

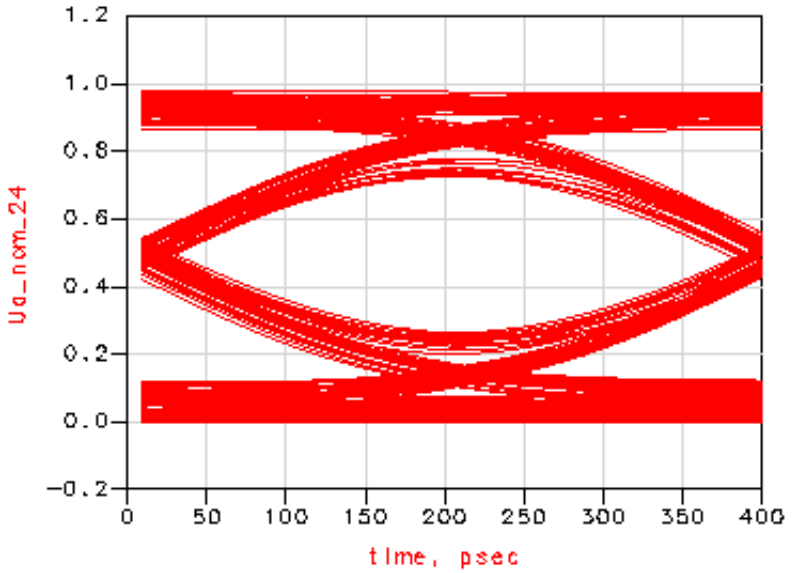
freq	S11_dB	S11_lin
1.20GHz	−8.42	0.38
2.40GHz	−4.47	0.60
3.60GHz	−3.74	0.65
4.80GHz	−2.84	0.72

Transmission S21

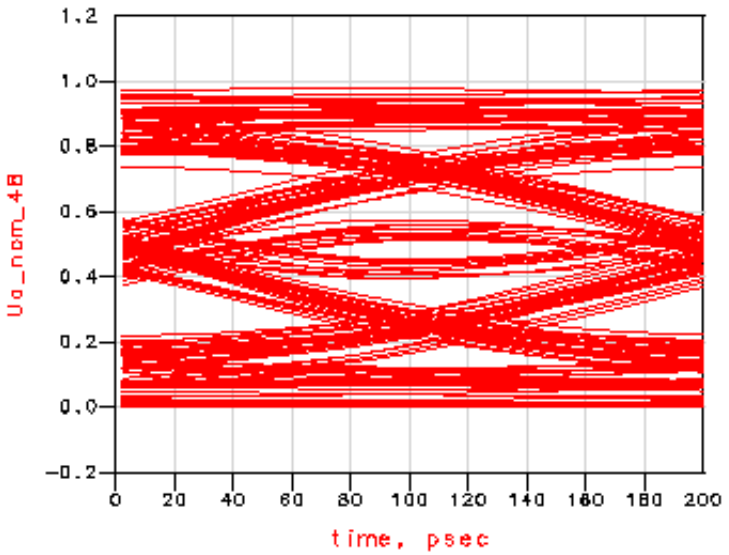
freq	S21_dB	S21_lin
1.20GHz	−5.99	0.50
2.40GHz	−14.00	0.20
3.60GHz	−25.23	0.05
4.80GHz	−44.13	0.01



Impedance of transmission path

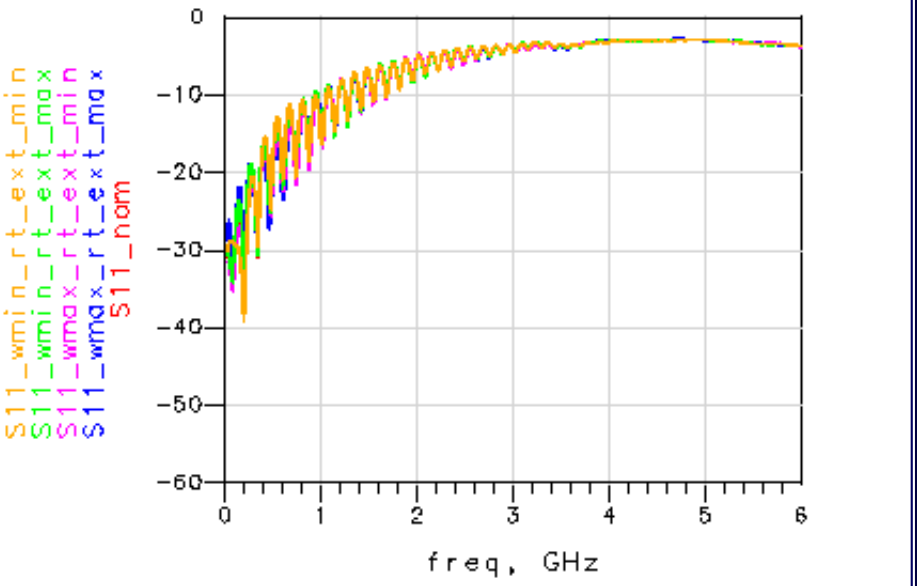


System eye diagram @ 2.4 GBit/s

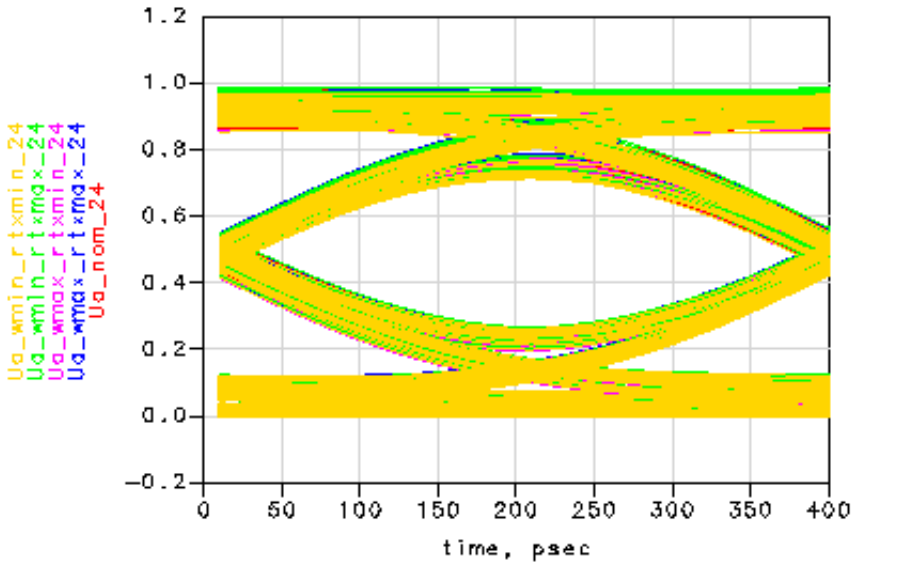


System eye diagram @ 4.8 GBit/s

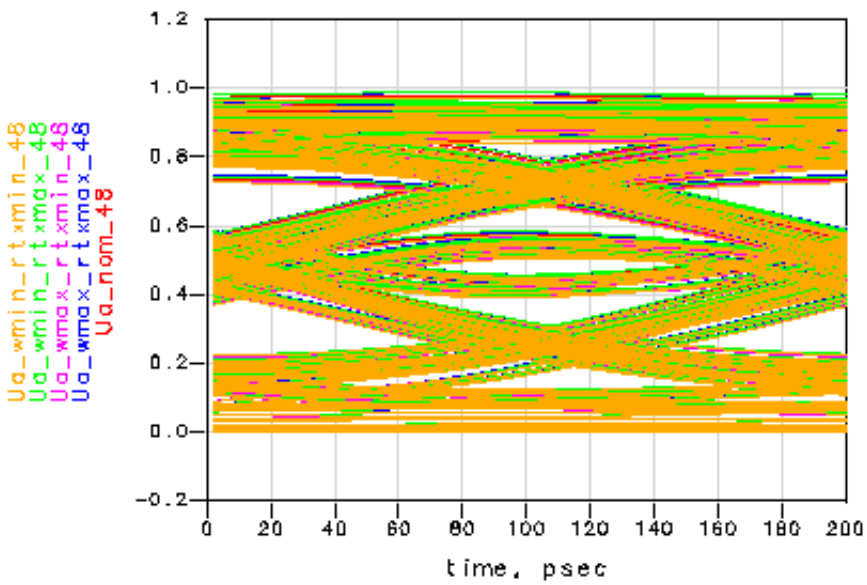
Tolerance analysis with external resistors (+/- 2%)



Input reflection S11

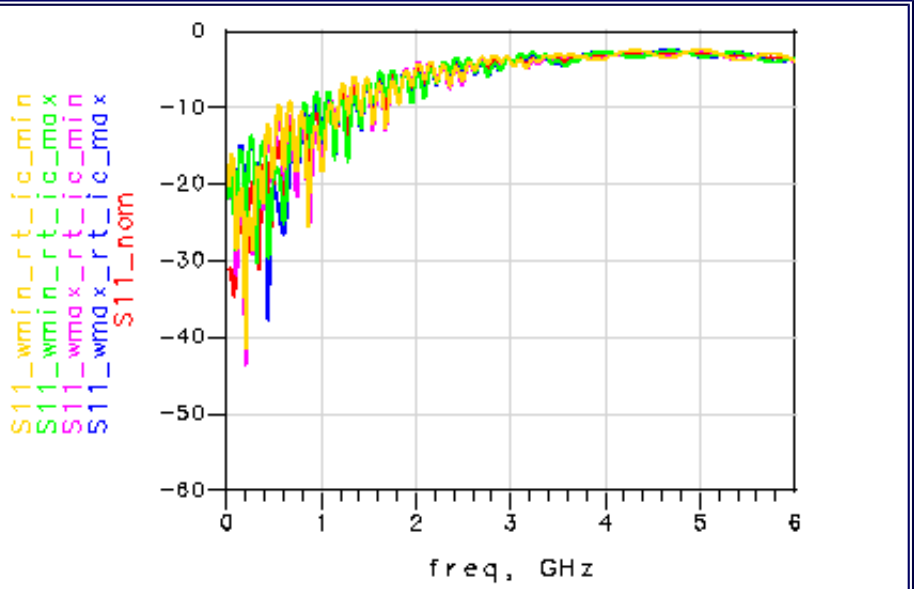


System eye diagram @ 2.4 GBit/s

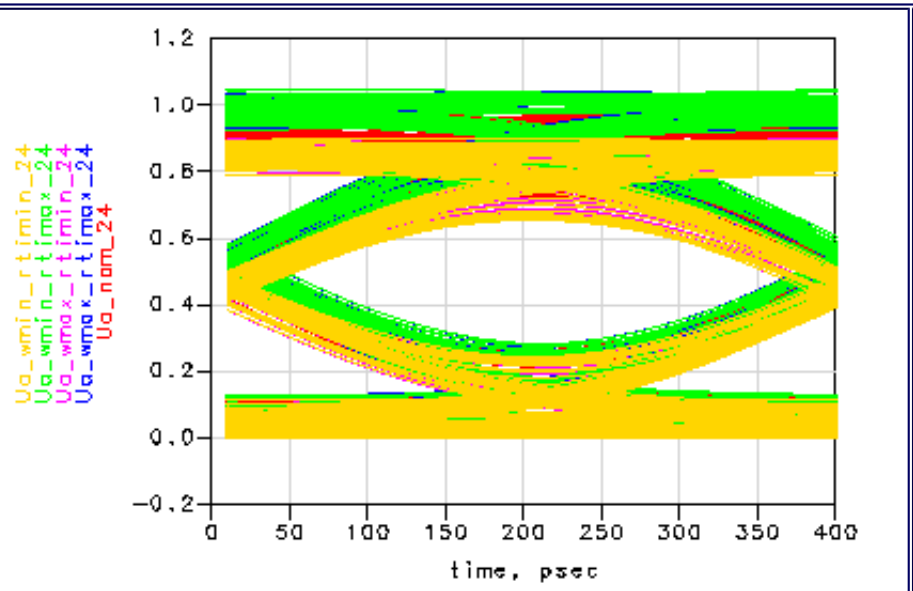


System eye diagram @ 4.8 GBit/s

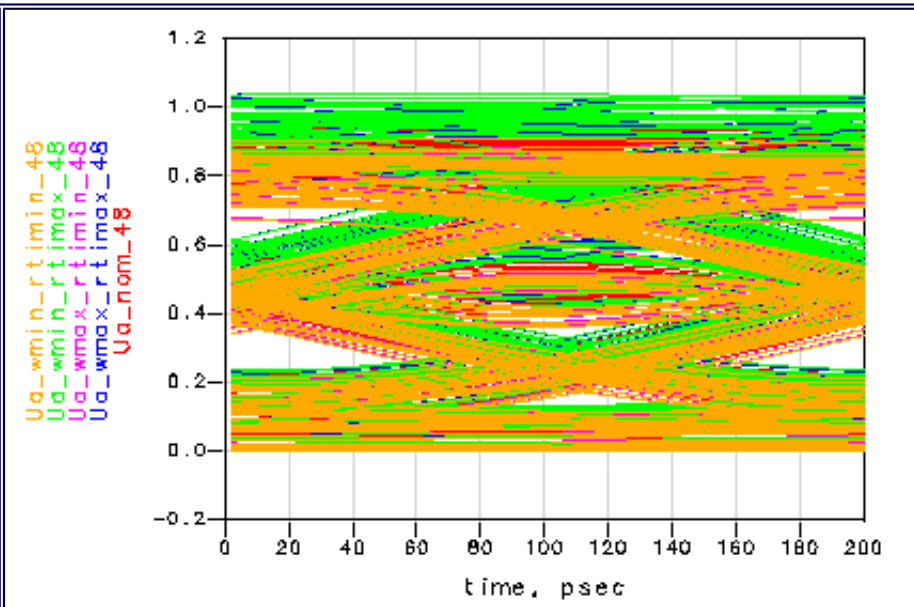
Tolerance analysis with on-chip termination resistors (+/- 15%)



Input reflection S11



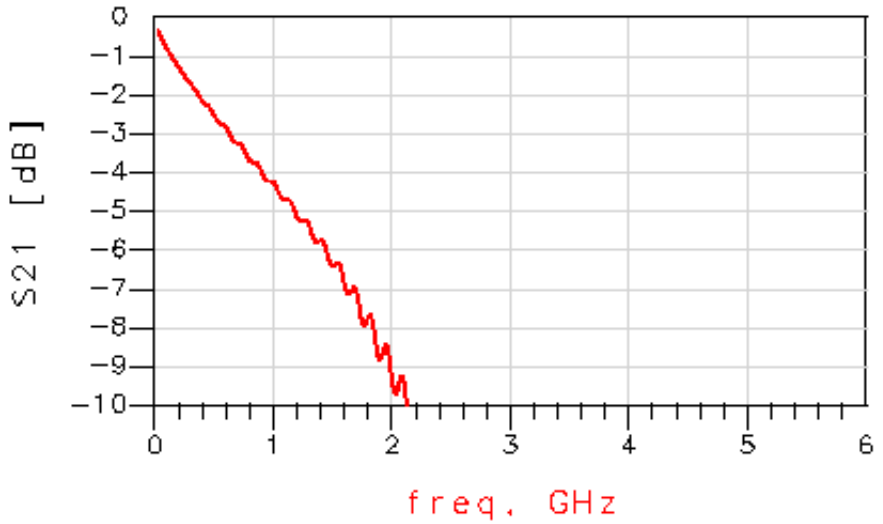
System eye diagram @ 2.4 GBit/s



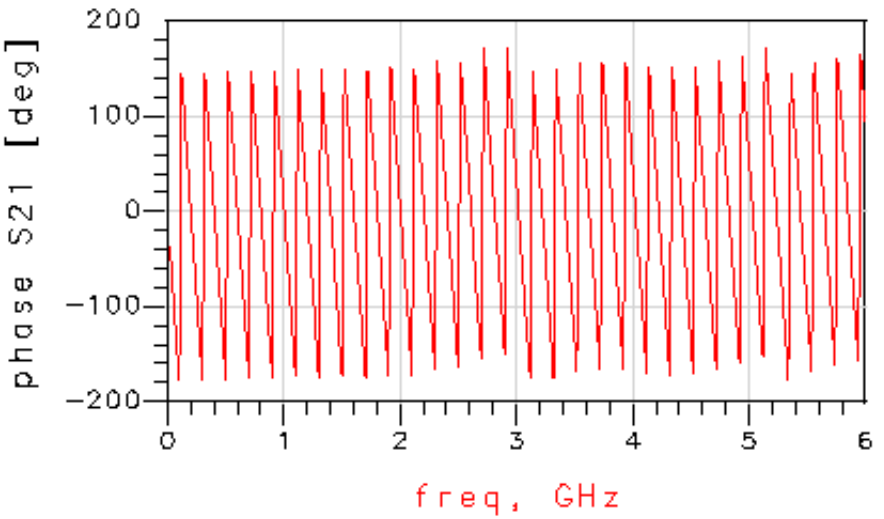
System eye diagram @ 4.8 GBit/s

	Connector to board interface		PCB	Backplane			
Simulation run	Backplane	Daughter-card	Material	Trace length [mm]	Trace width [mm]	Backplane transmission line type	Layer of transmission line
3	PF	PF	FR4	500	0.15	stripline	bottom

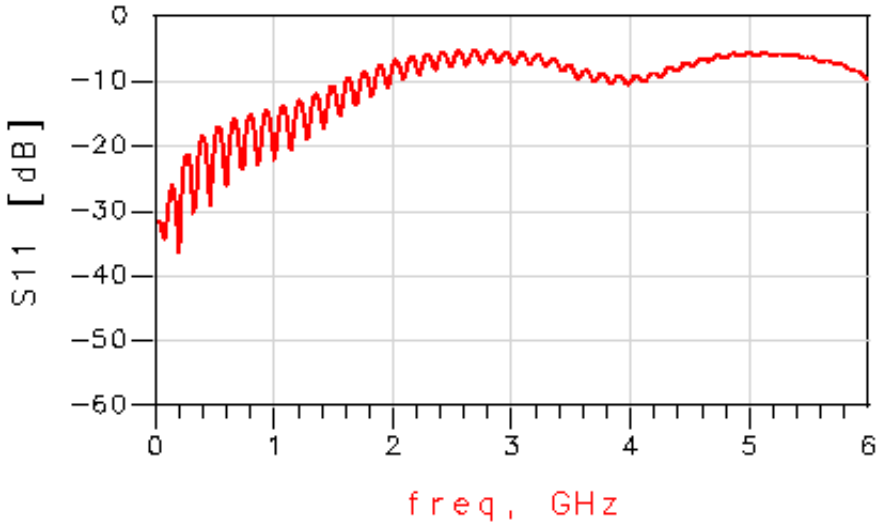
Nominal results



Magnitude of forward transmission S21



Phase of forward transmission S21



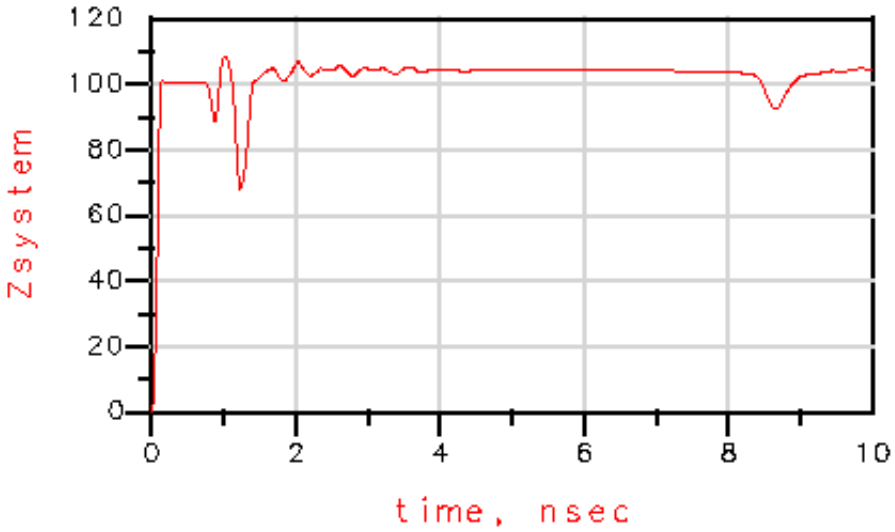
Input reflection S11

Input reflection S11

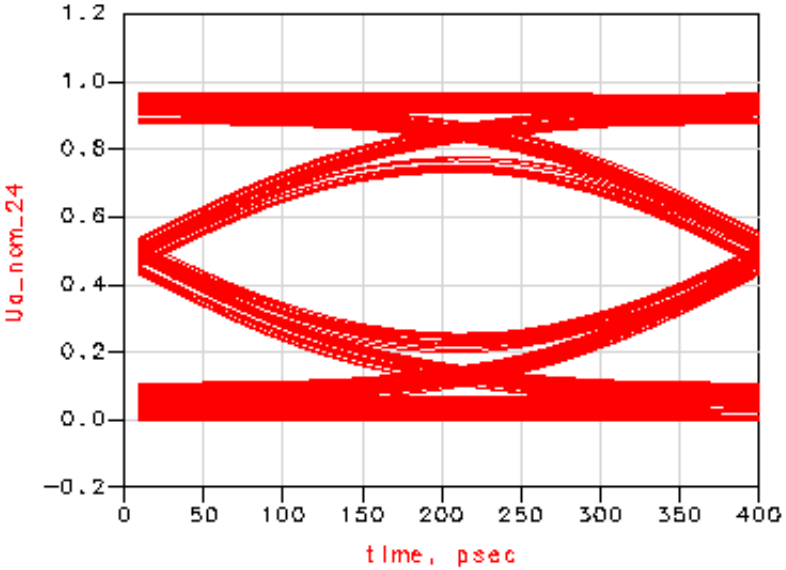
freq	S11_dB	S11_lin
1.20GHz	−13.19	0.22
2.40GHz	−5.85	0.51
3.60GHz	−8.61	0.37
4.80GHz	−6.33	0.48

Transmission S21

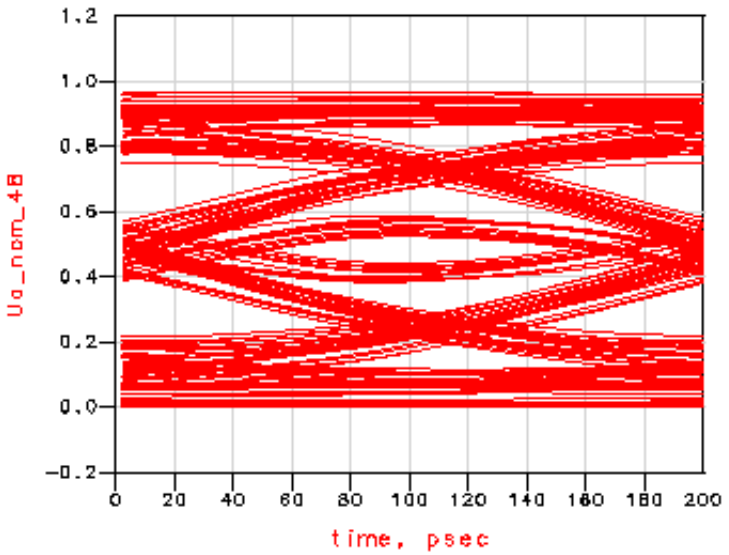
freq	S21_dB	S21_lin
1.20GHz	−5.15	0.55
2.40GHz	−12.02	0.25
3.60GHz	−15.16	0.17
4.80GHz	−20.06	0.10



Impedance of transmission path

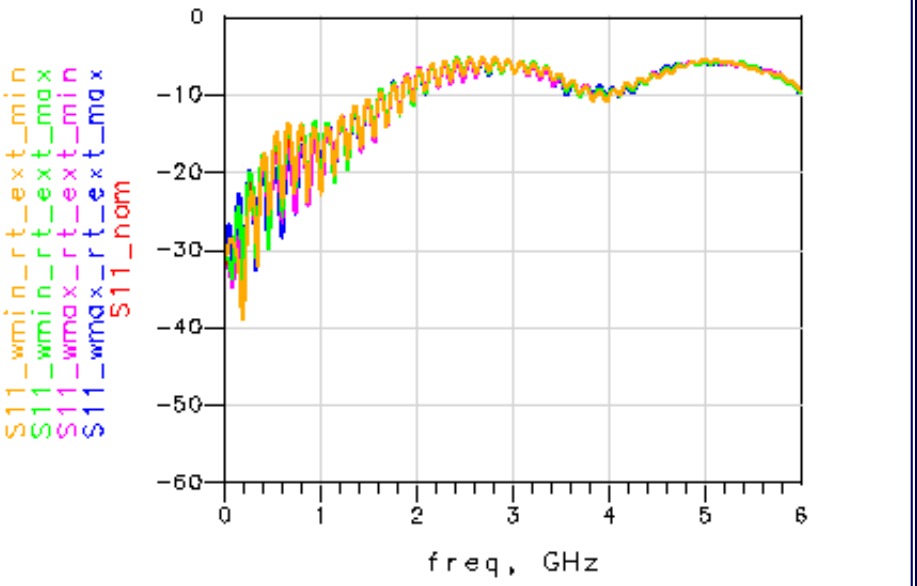


System eye diagram @ 2.4 GBit/s

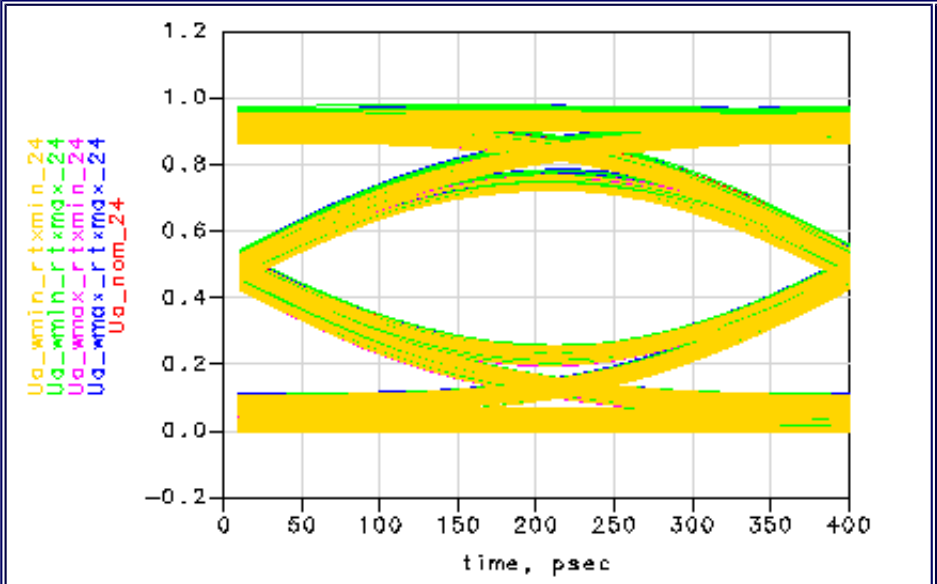


System eye diagram @ 4.8 GBit/s

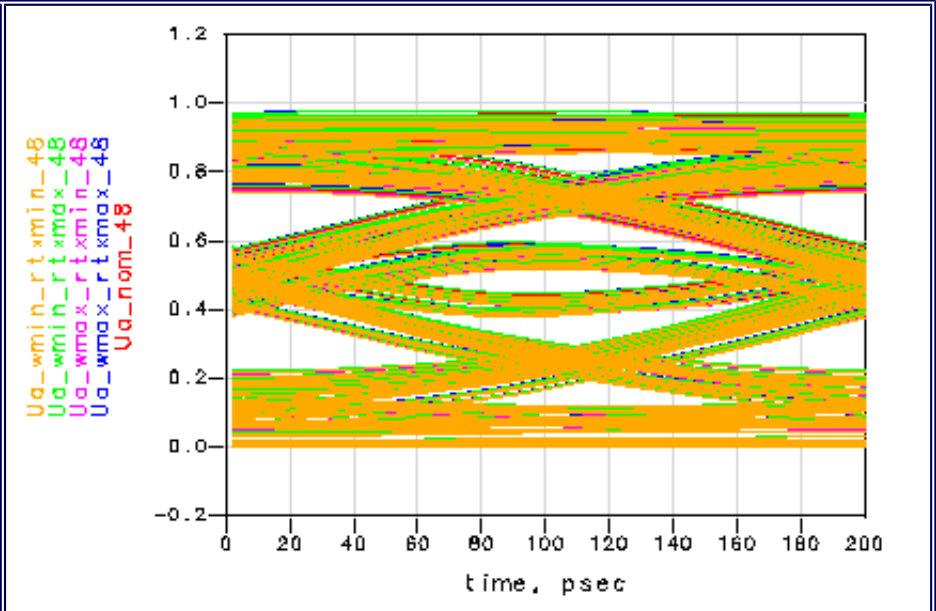
Tolerance analysis with external resistors (+/- 2%)



Input reflection S11

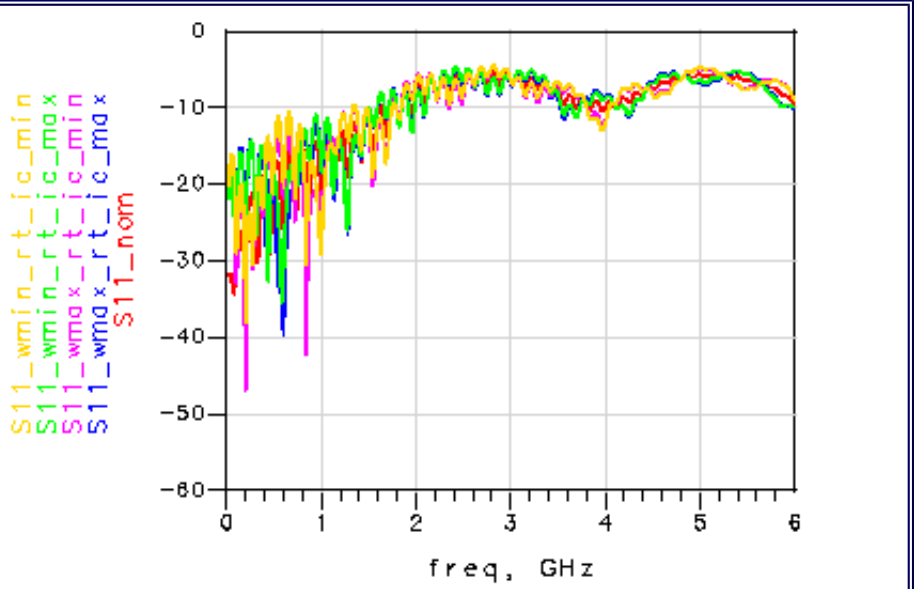


System eye diagram @ 2.4 GBit/s

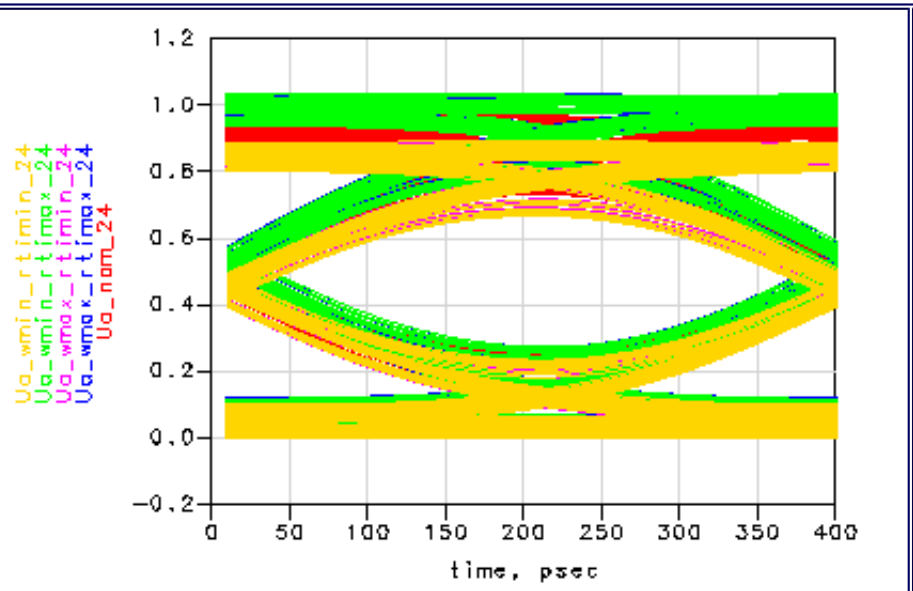


System eye diagram @ 4.8 GBit/s

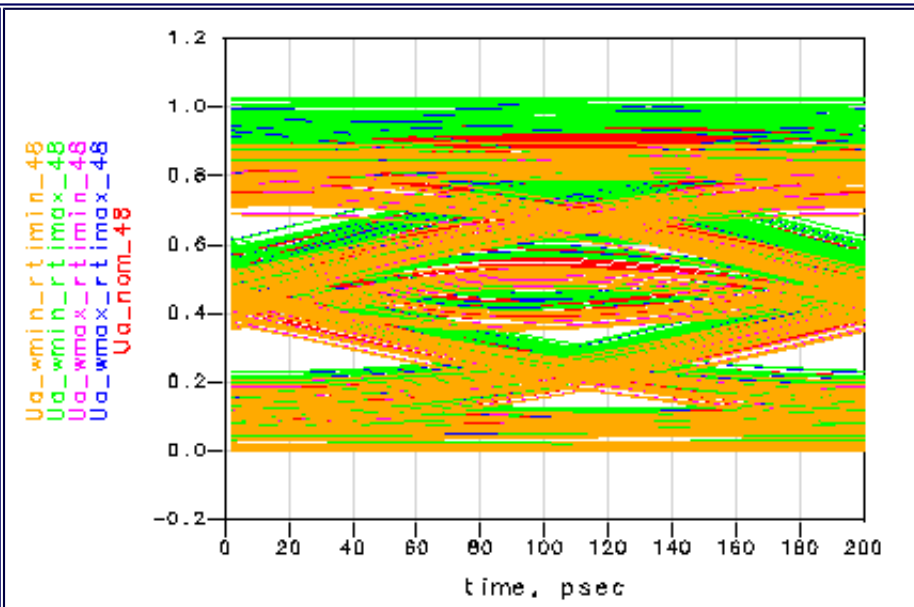
Tolerance analysis with on-chip termination resistors (+/- 15%)



Input reflection S11



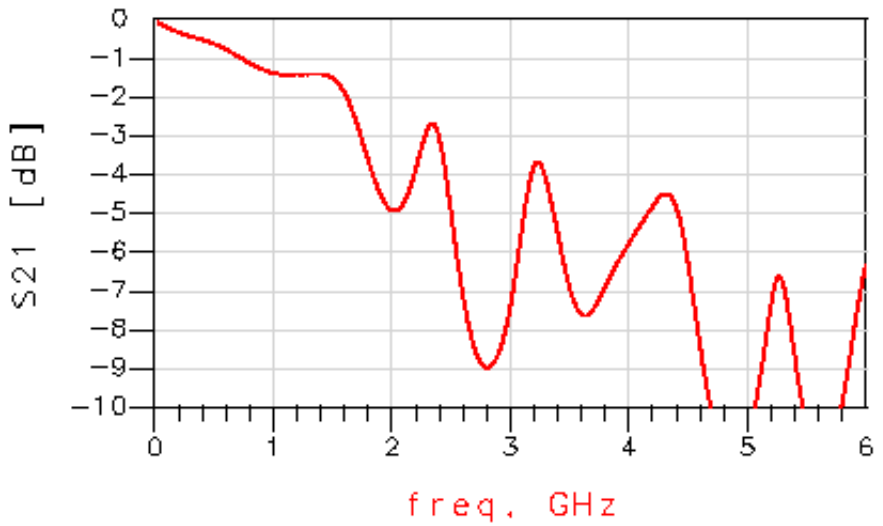
System eye diagram @ 2.4 GBit/s



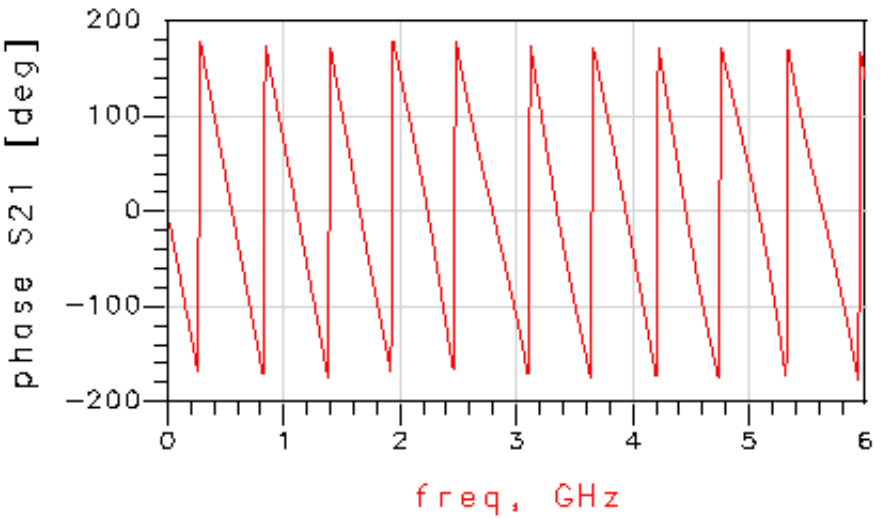
System eye diagram @ 4.8 GBit/s

	Connector to board interface		PCB	Backplane			
Simulation run	Backplane	Daughter-card	Material	Trace length [mm]	Trace width [mm]	Backplane transmission line type	Layer of transmission line
11	PF	PF	FR4	50	0.15	stripline	bottom

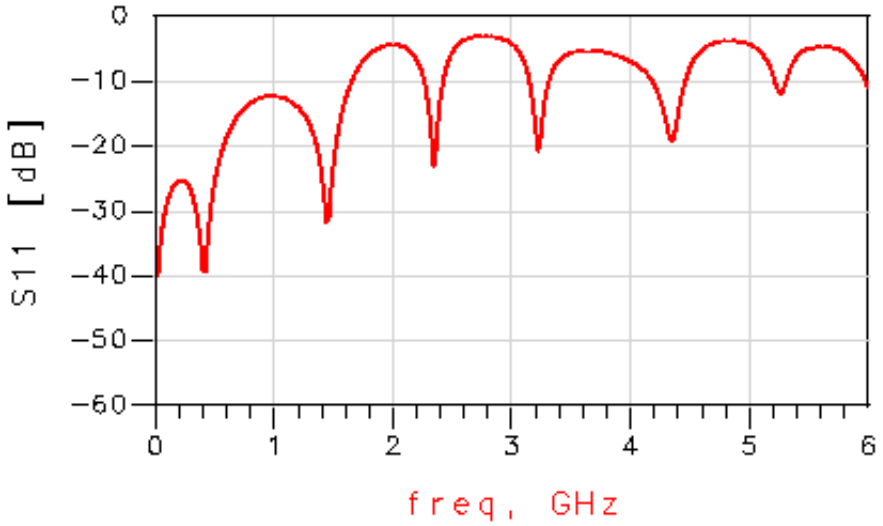
Nominal results



Magnitude of forward transmission S21



Phase of forward transmission S21



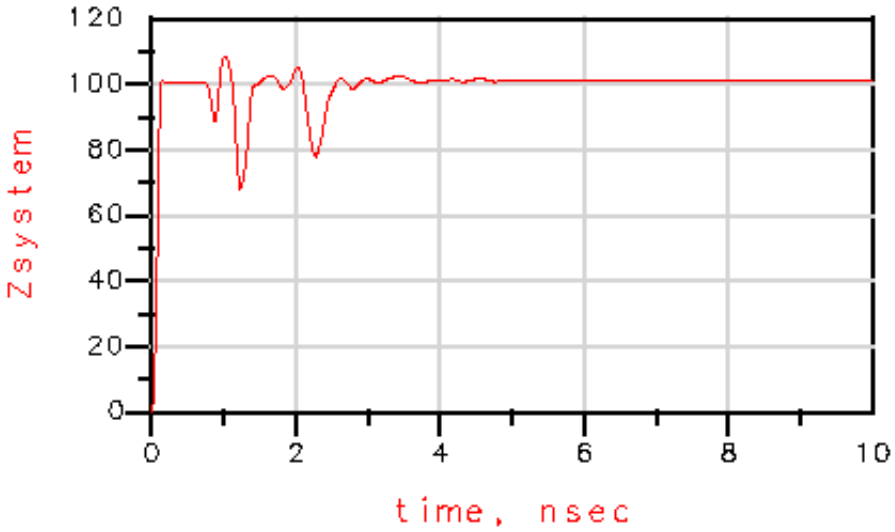
Input reflection S11

Input reflection S11

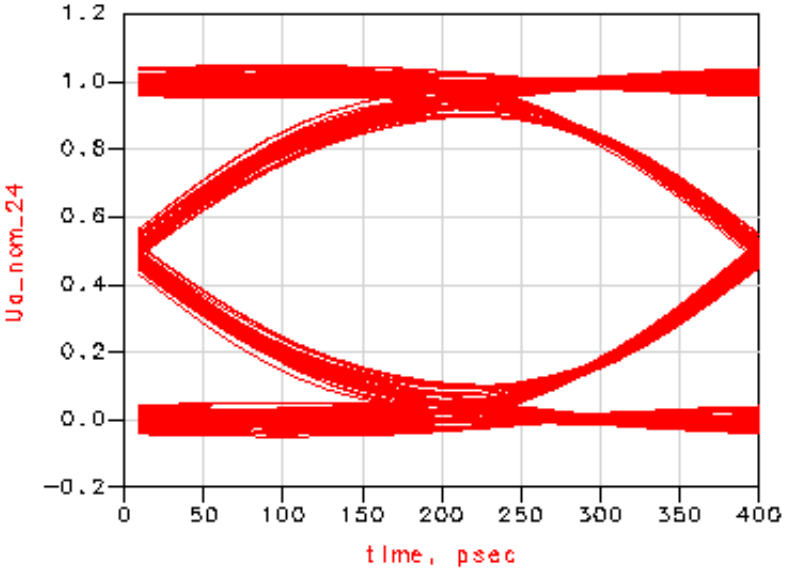
freq	S11_dB	S11_lin
1.20GHz	−14.01	0.20
2.40GHz	−12.57	0.24
3.60GHz	−5.31	0.54
4.80GHz	−3.78	0.65

Transmission S21

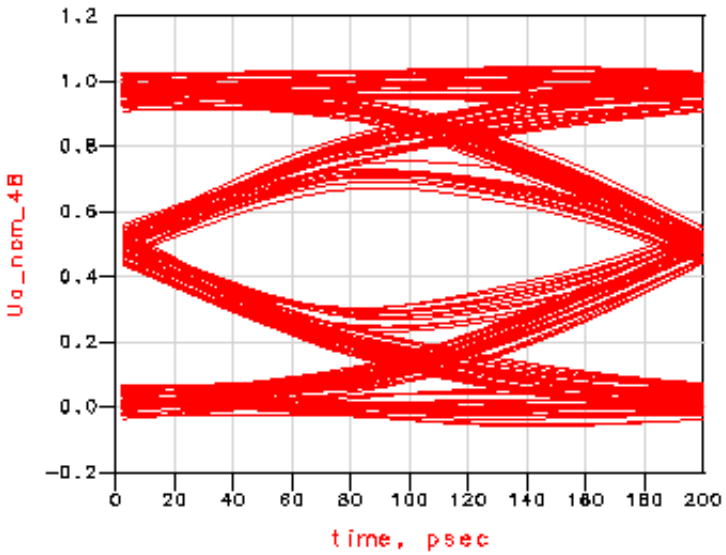
freq	S21_dB	S21_lin
1.20GHz	−1.44	0.85
2.40GHz	−3.05	0.70
3.60GHz	−7.61	0.42
4.80GHz	−11.26	0.27



Impedance of transmission path

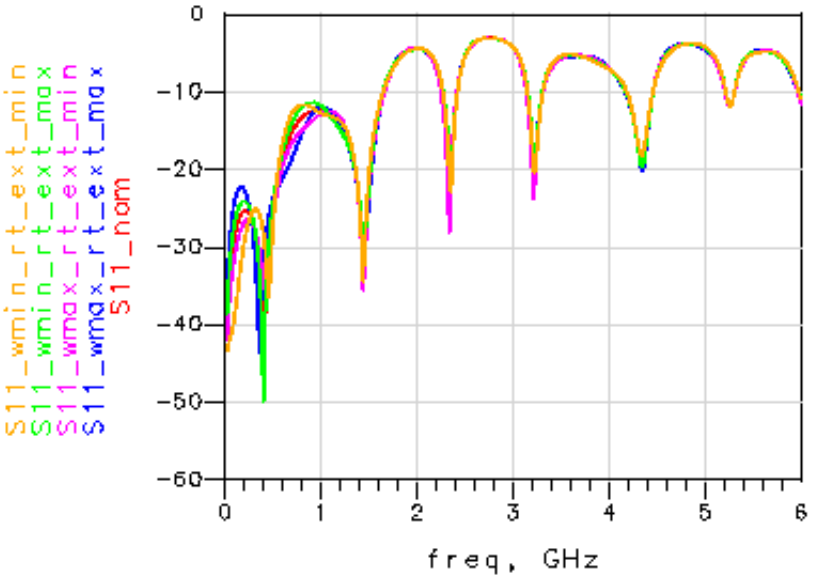


System eye diagram @ 2.4 GBit/s

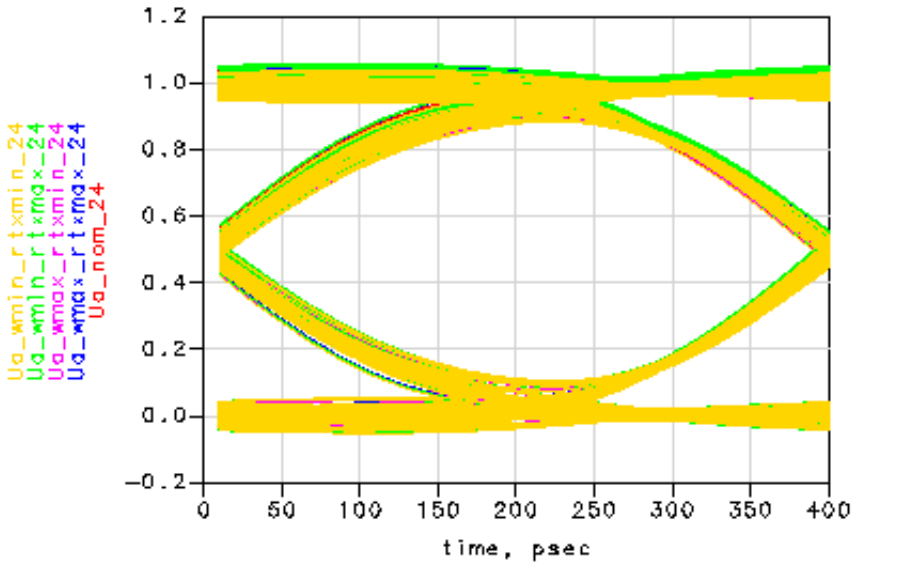


System eye diagram @ 4.8 GBit/s

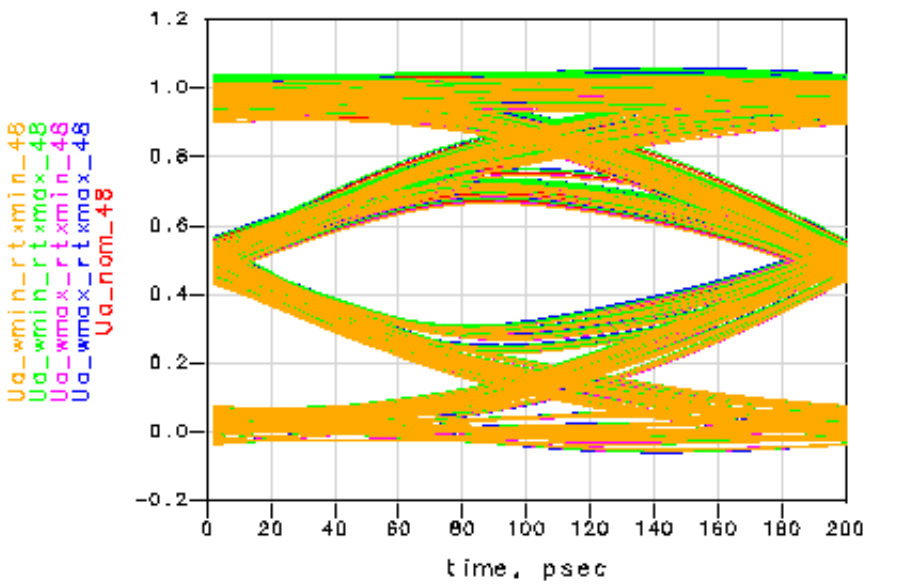
Tolerance analysis with external resistors (+/- 2%)



Input reflection S11

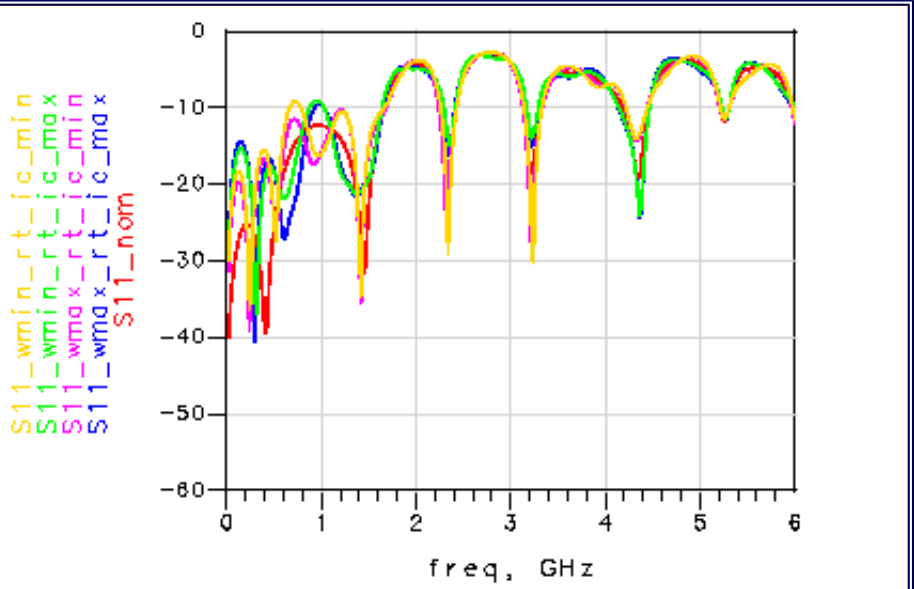


System eye diagram @ 2.4 GBit/s

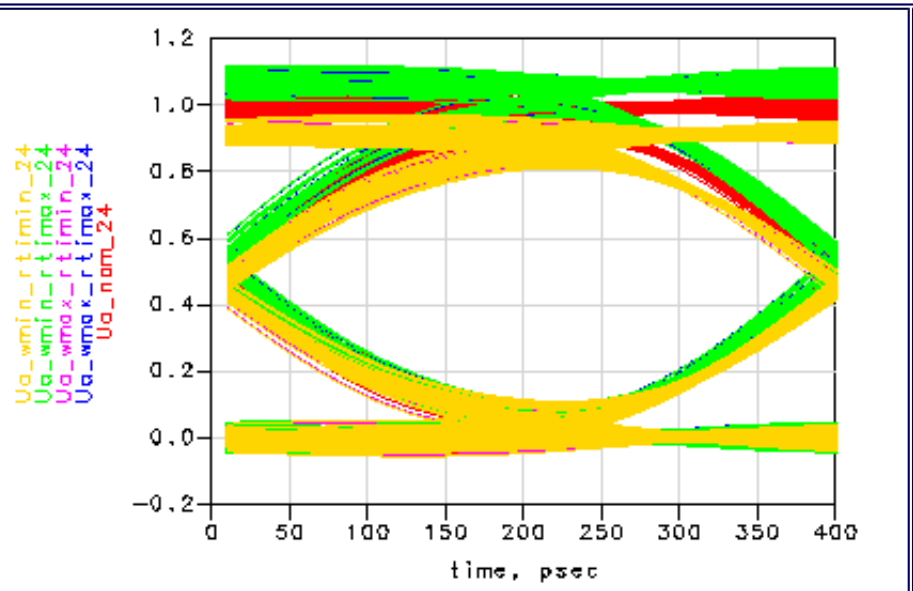


System eye diagram @ 4.8 GBit/s

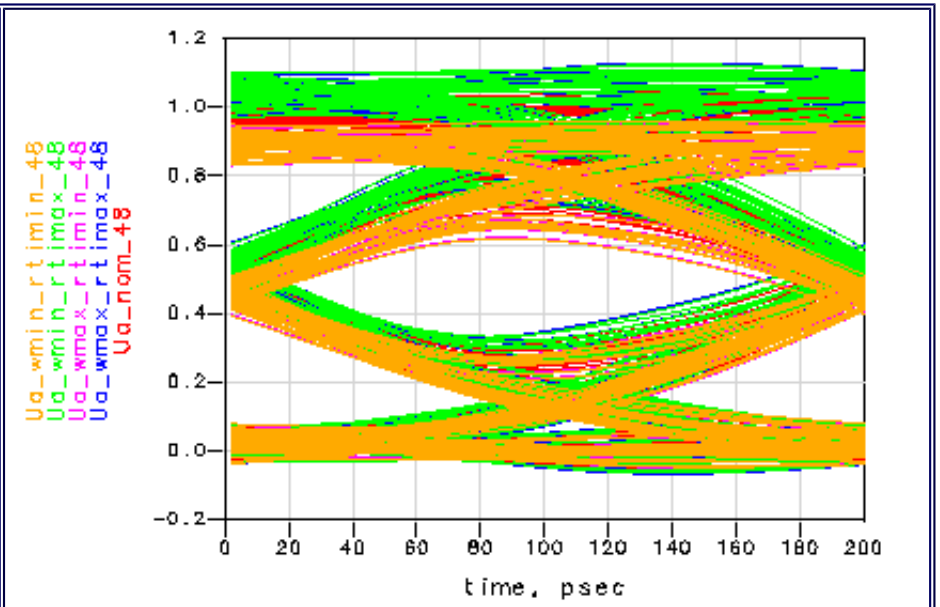
Tolerance analysis with on-chip termination resistors (+/- 15%)



Input reflection S11



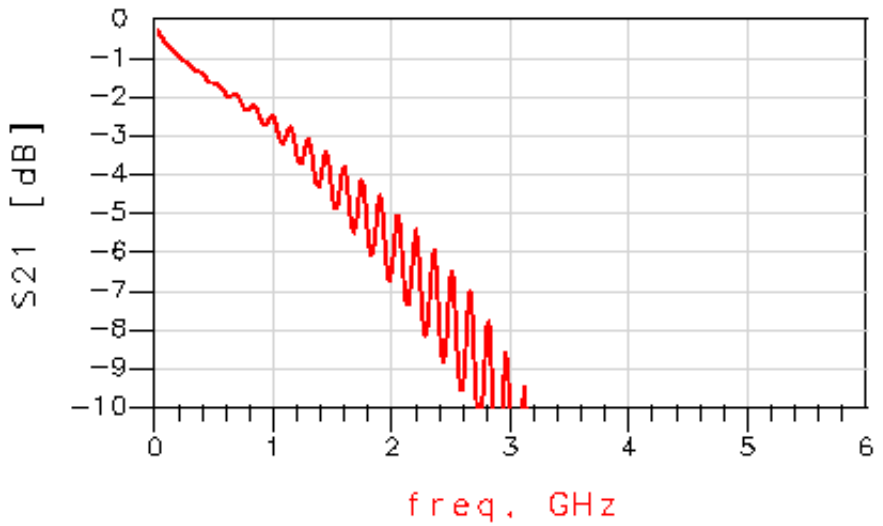
System eye diagram @ 2.4 GBit/s



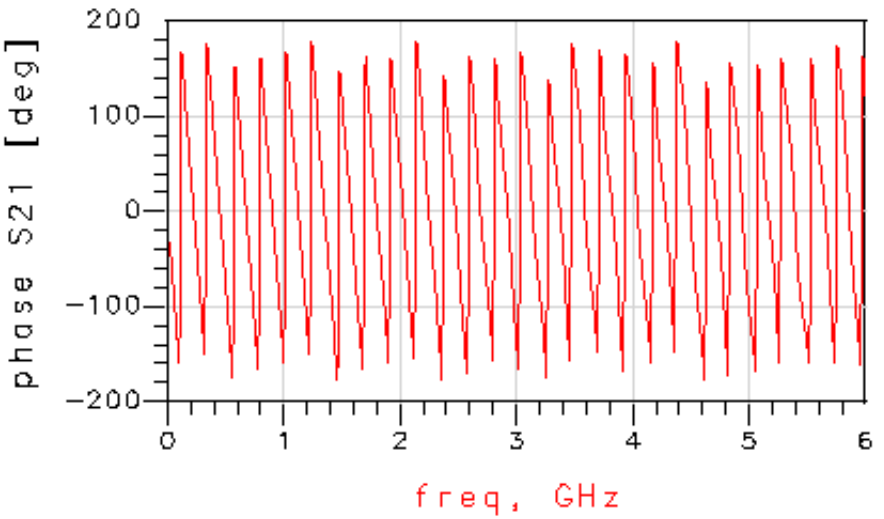
System eye diagram @ 4.8 GBit/s

	Connector to board interface		PCB	Backplane			
Simulation run	Backplane	Daughter-card	Material	Trace length [mm]	Trace width [mm]	Backplane transmission line type	Layer of transmission line
18	PF	SMD	Rogers	500	0.15	stripline	top

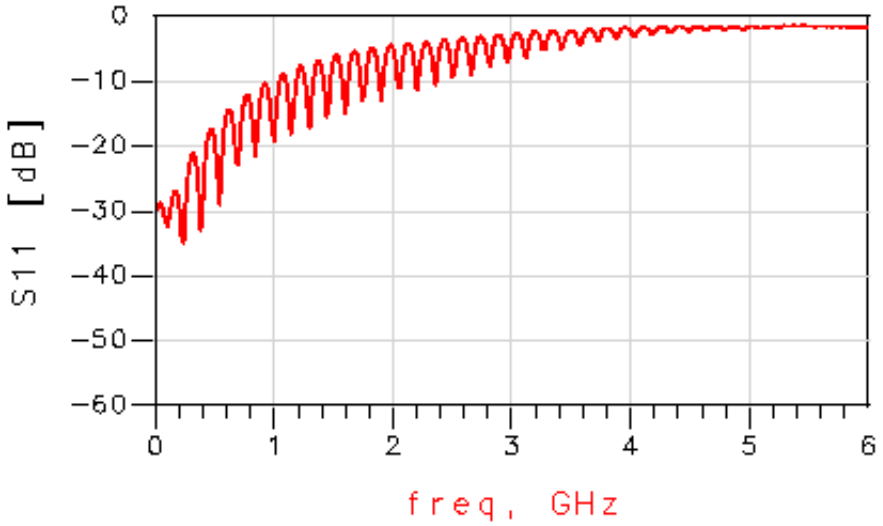
Nominal results



Magnitude of forward transmission S21



Phase of forward transmission S21



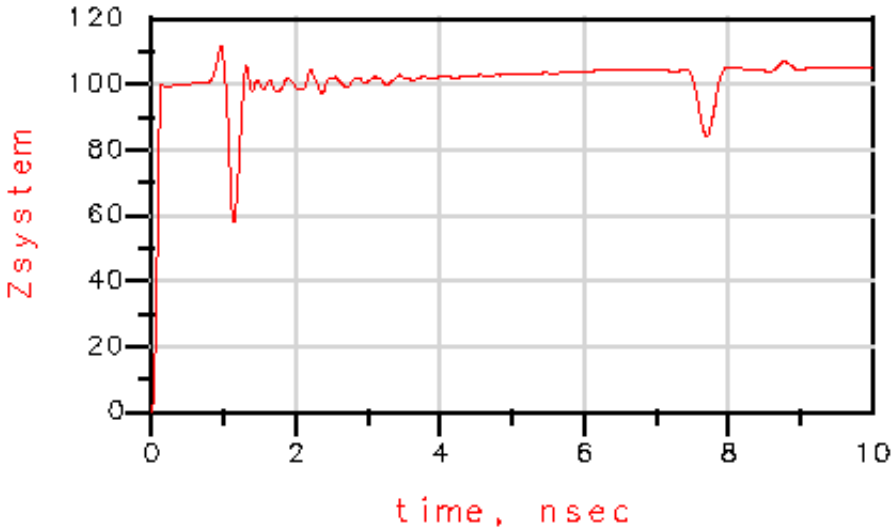
Input reflection S11

Input reflection S11

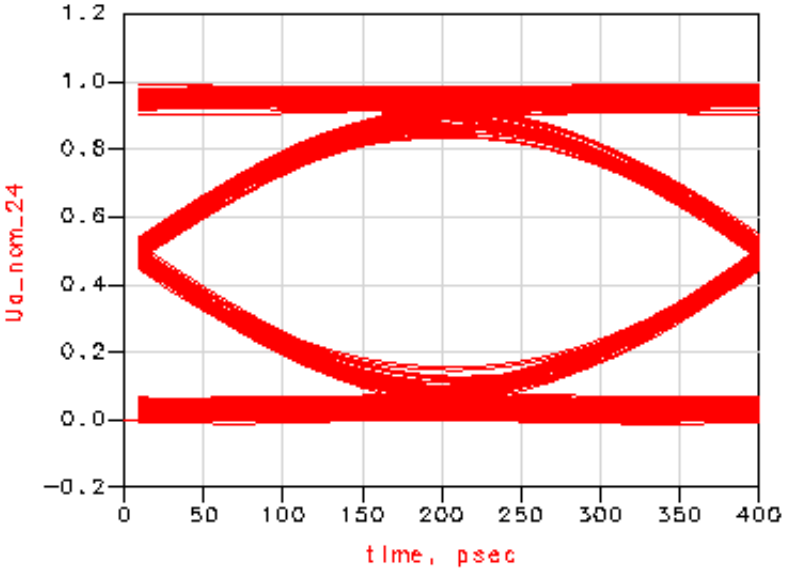
freq	S11_dB	S11_lin
1.20GHz	−8.47	0.38
2.40GHz	−4.62	0.59
3.60GHz	−3.18	0.69
4.80GHz	−2.05	0.79

Transmission S21

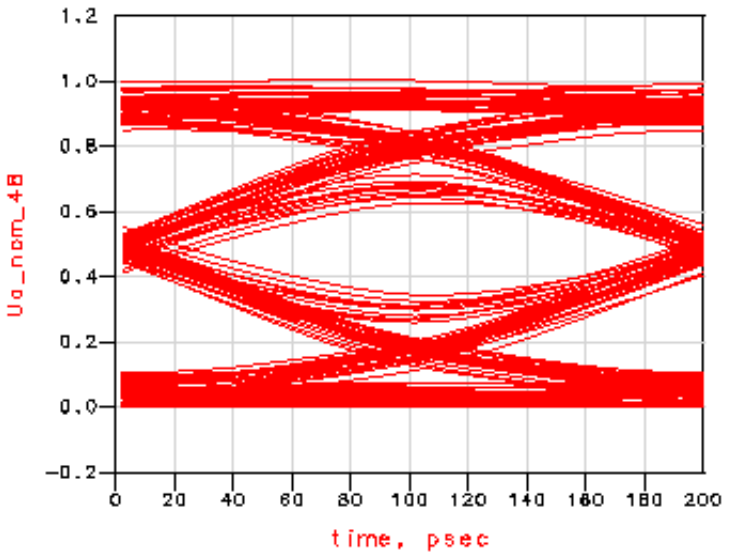
freq	S21_dB	S21_lin
1.20GHz	−3.53	0.67
2.40GHz	−7.86	0.40
3.60GHz	−14.72	0.18
4.80GHz	−24.56	0.06



Impedance of transmission path

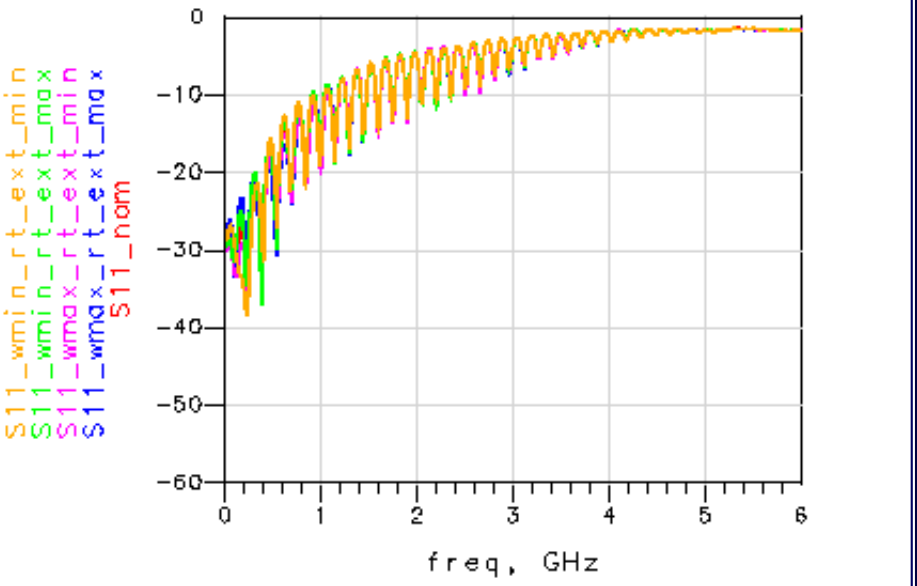


System eye diagram @ 2.4 GBit/s

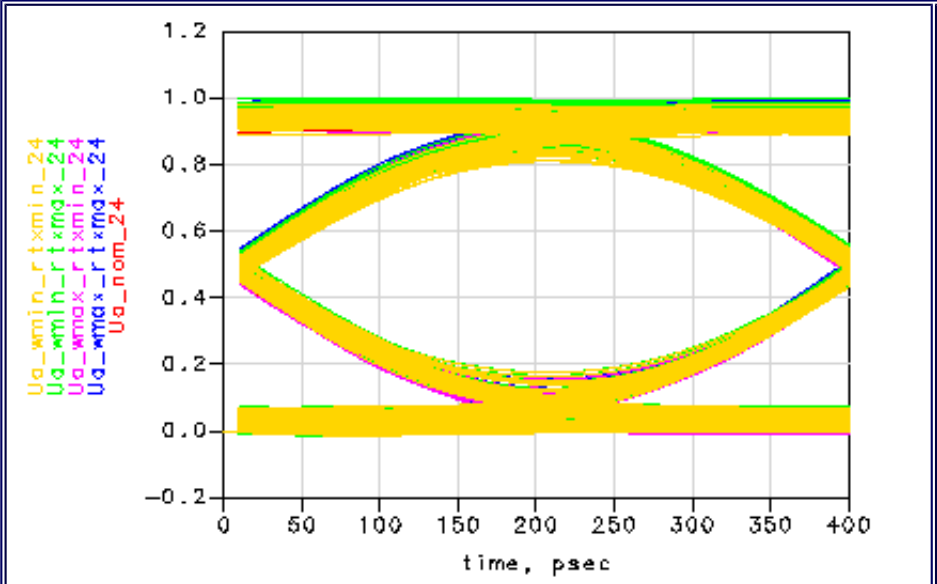


System eye diagram @ 4.8 GBit/s

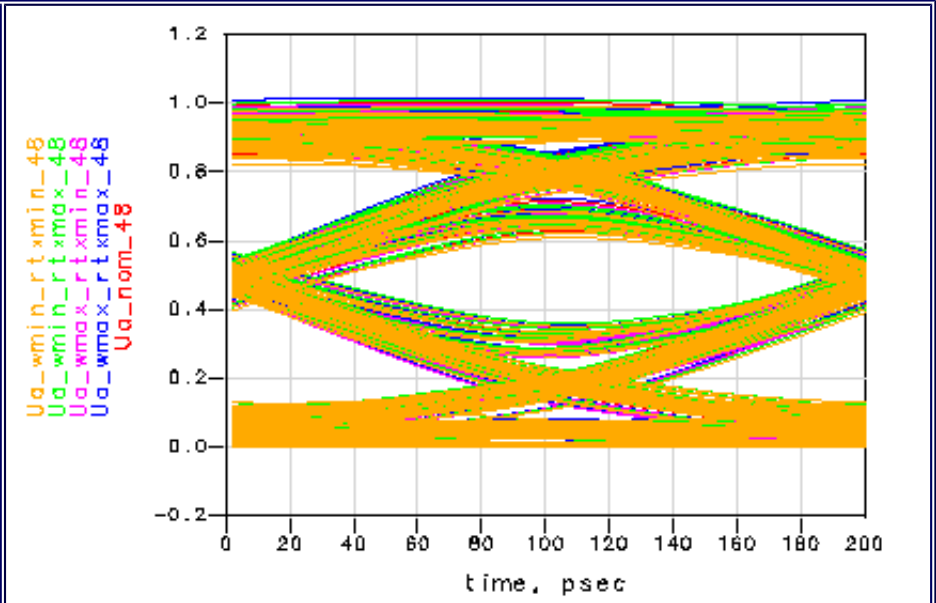
Tolerance analysis with external resistors (+/- 2%)



Input reflection S11

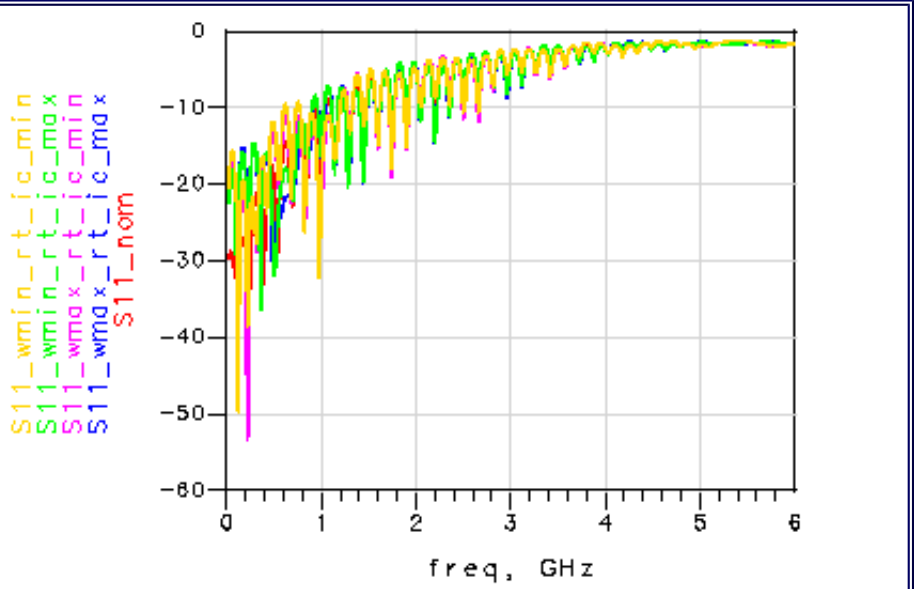


System eye diagram @ 2.4 GBit/s

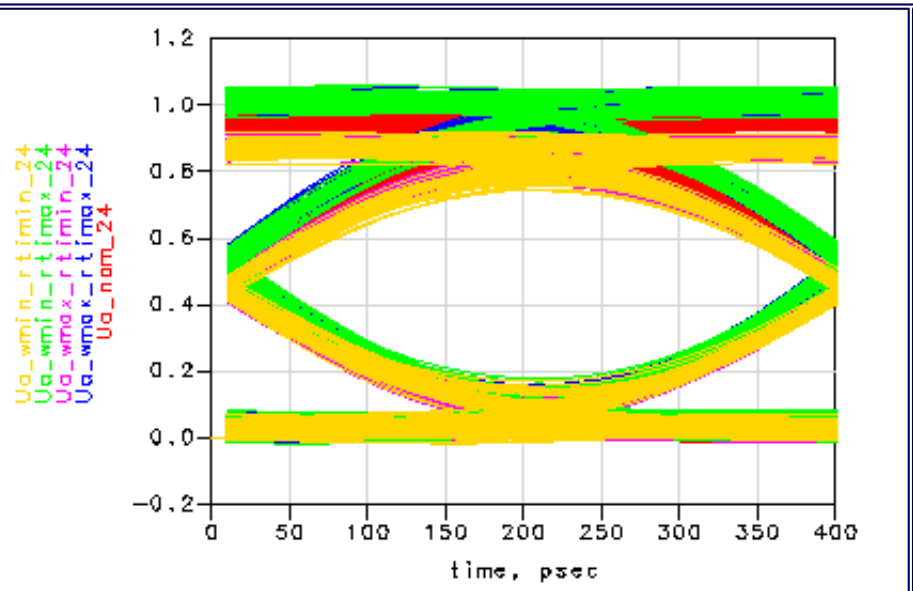


System eye diagram @ 4.8 GBit/s

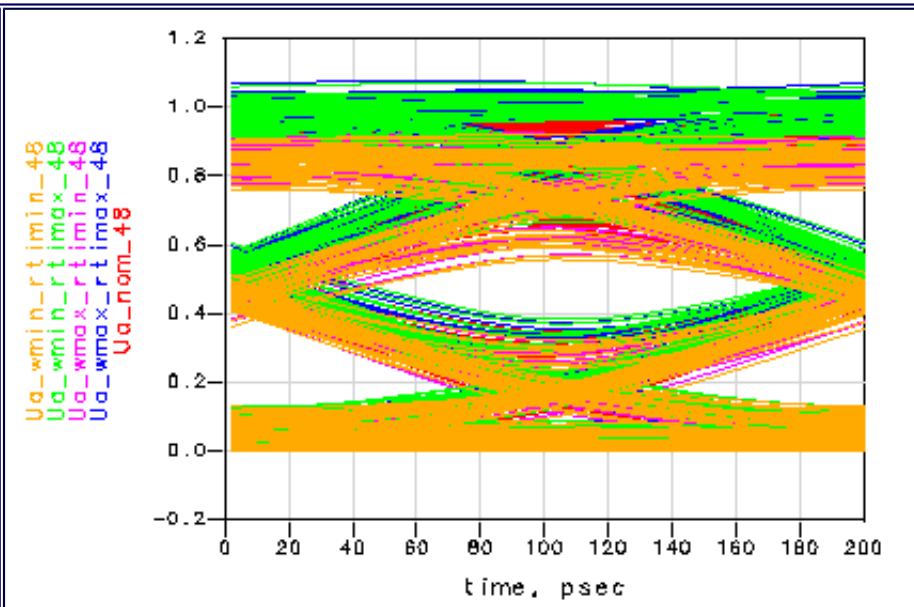
Tolerance analysis with on-chip termination resistors (+/- 15%)



Input reflection S11



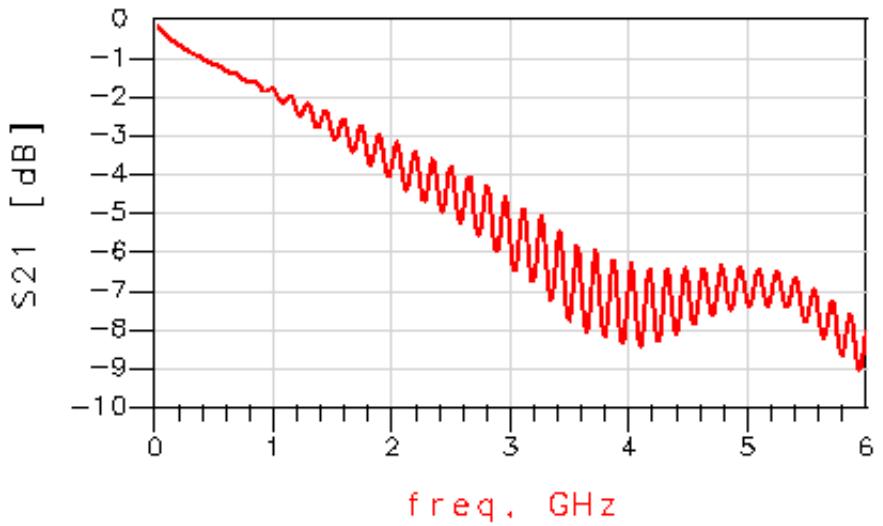
System eye diagram @ 2.4 GBit/s



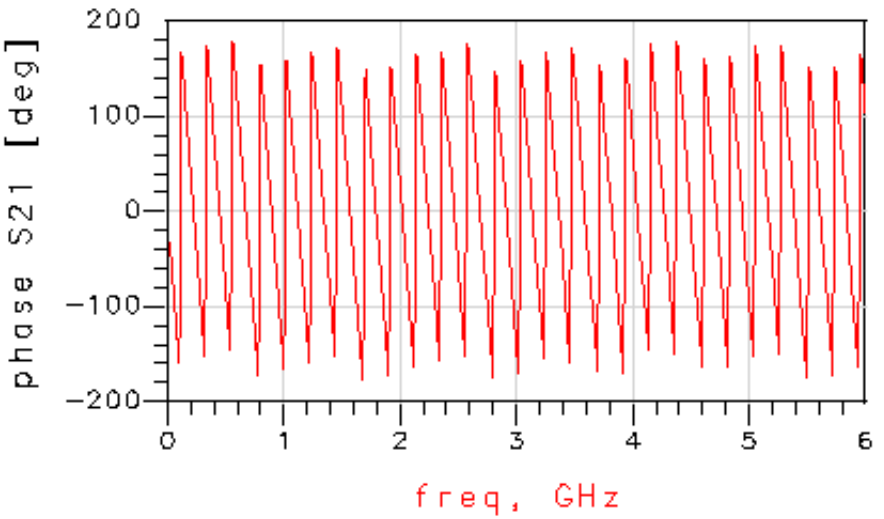
System eye diagram @ 4.8 GBit/s

	Connector to board interface		PCB	Backplane			
Simulation run	Backplane	Daughter-card	Material	Trace length [mm]	Trace width [mm]	Backplane transmission line type	Layer of transmission line
31	PF	SMD	Rogers	500	0.25	stripline	bottom

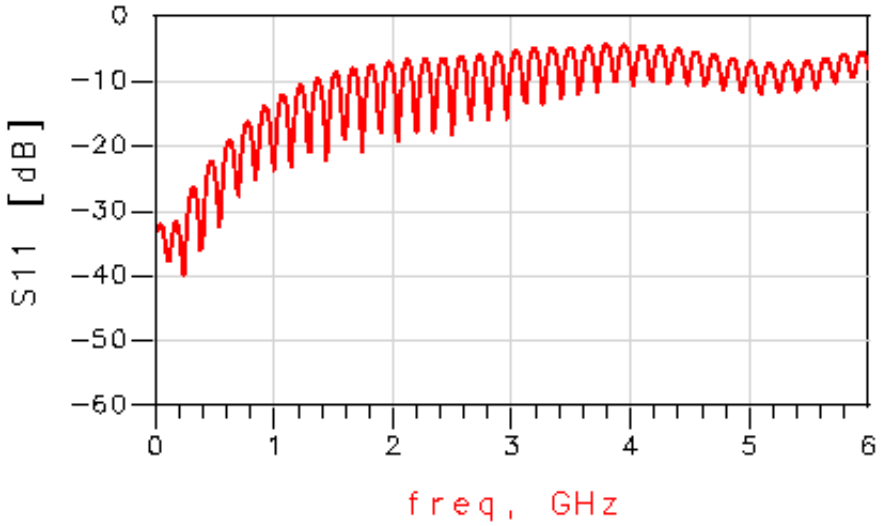
Nominal results



Magnitude of forward transmission S21



Phase of forward transmission S21



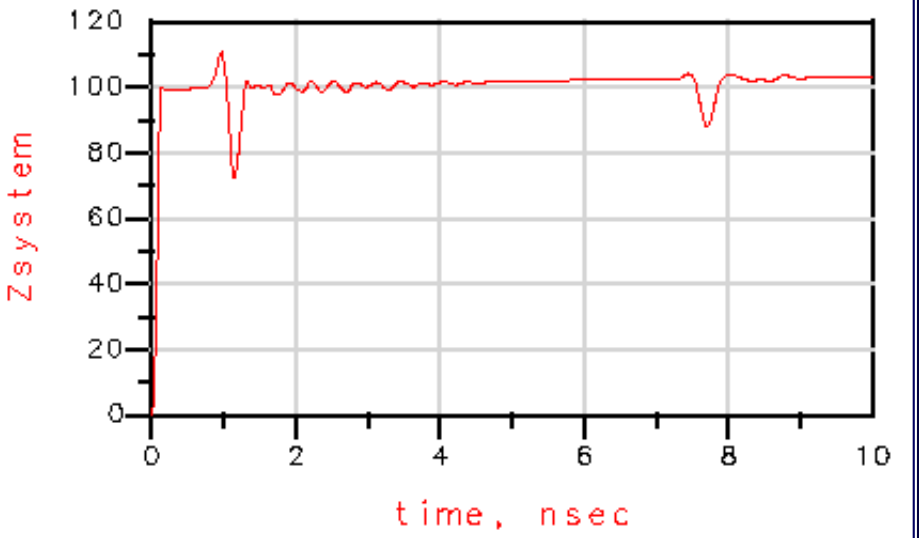
Input reflection S11

Input reflection S11

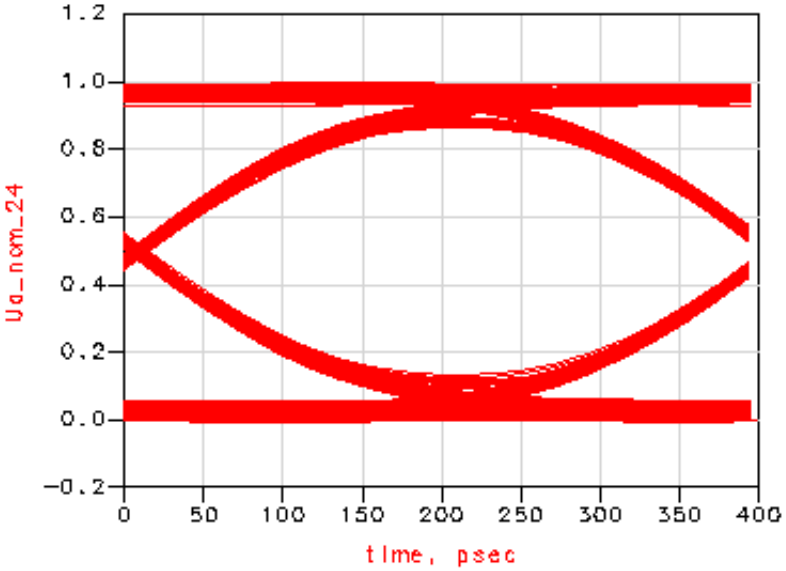
freq	S11_dB	S11_lin
1.20GHz	−11.24	0.27
2.40GHz	−7.09	0.44
3.60GHz	−6.88	0.45
4.80GHz	−10.13	0.31

Transmission S21

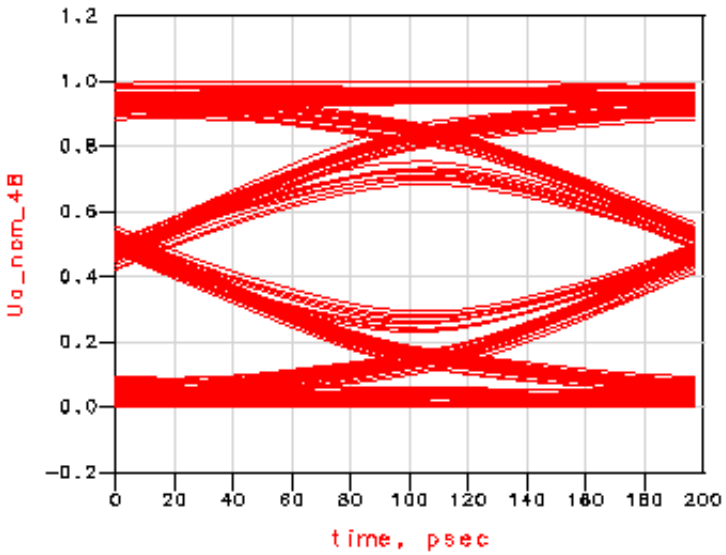
freq	S21_dB	S21_lin
1.20GHz	−2.38	0.76
2.40GHz	−4.70	0.58
3.60GHz	−6.86	0.45
4.80GHz	−6.48	0.47



Impedance of transmission path

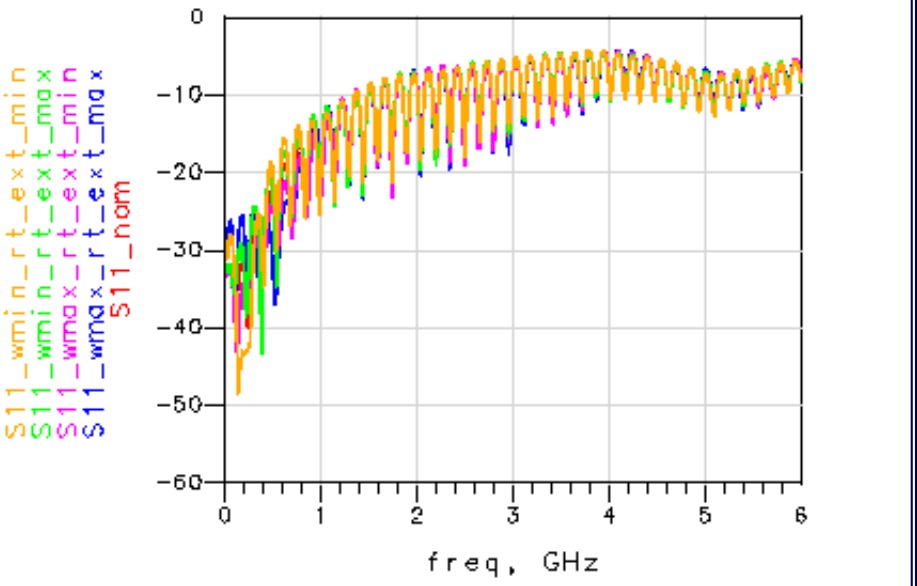


System eye diagram @ 2.4 GBit/s

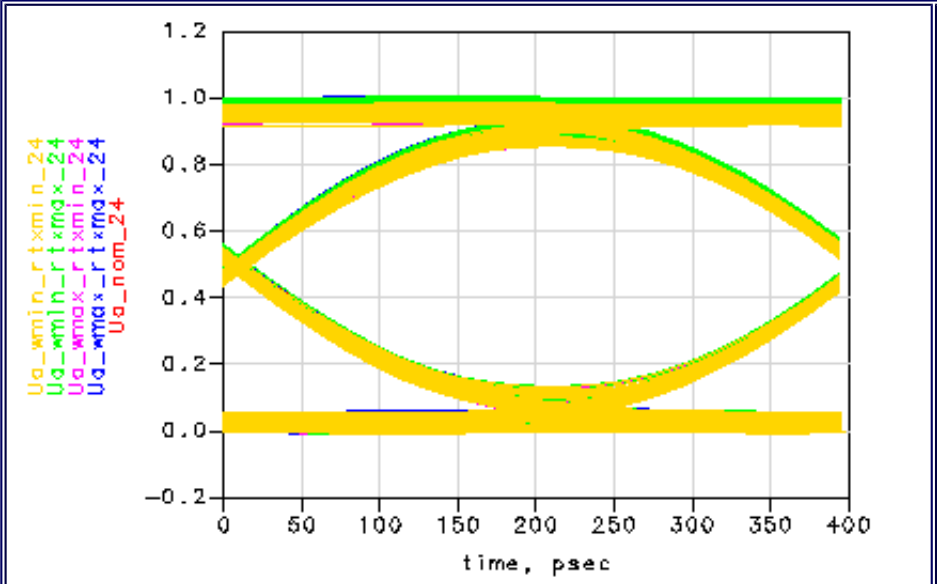


System eye diagram @ 4.8 GBit/s

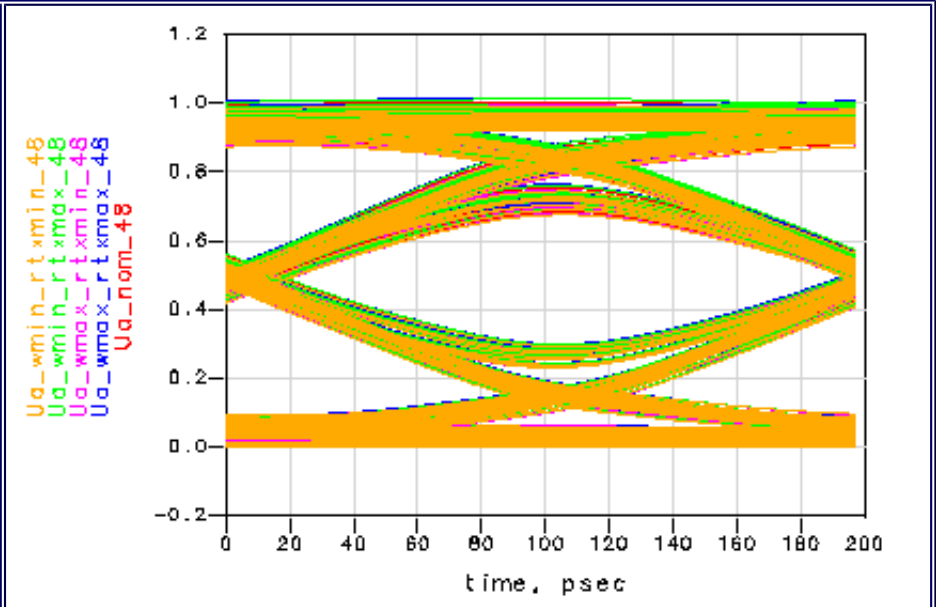
Tolerance analysis with external resistors (+/- 2%)



Input reflection S11

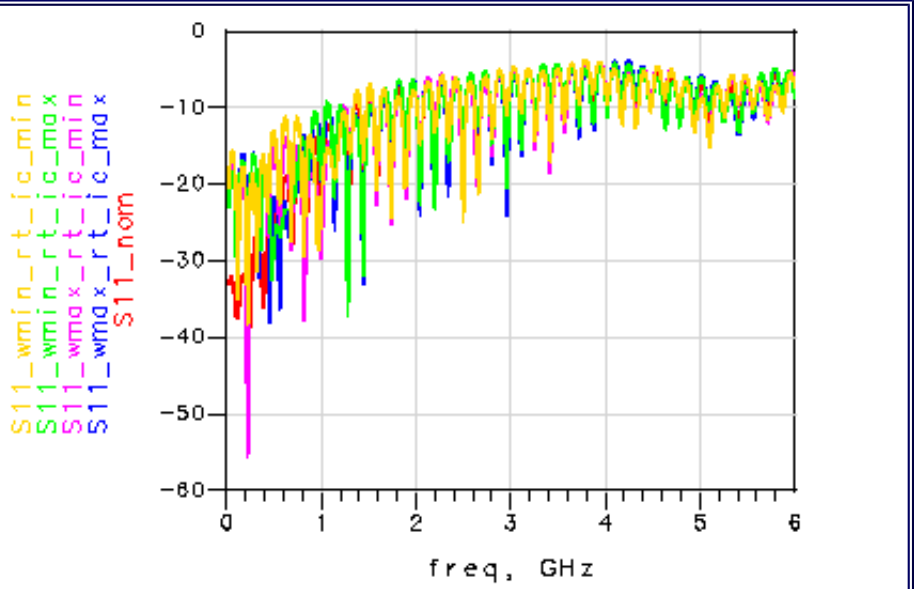


System eye diagram @ 2.4 GBit/s

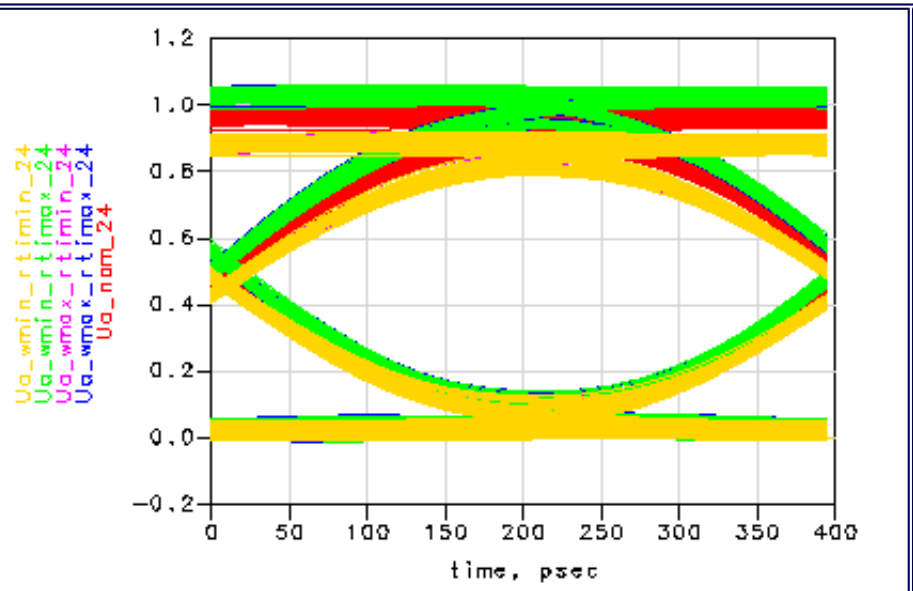


System eye diagram @ 4.8 GBit/s

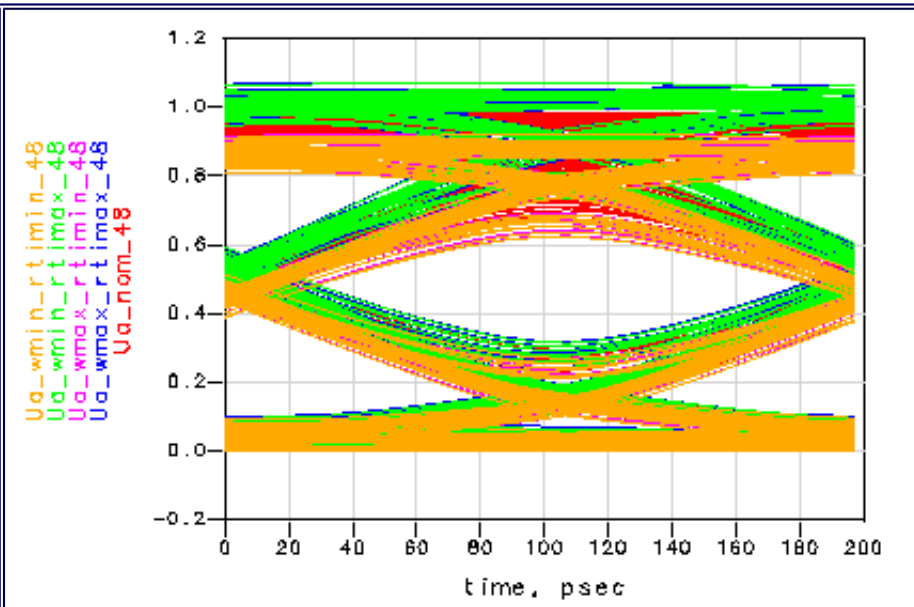
Tolerance analysis with on-chip termination resistors (+/- 15%)



Input reflection S11



System eye diagram @ 2.4 GBit/s



System eye diagram @ 4.8 GBit/s